Fraunhofer
IMS

FRAUNHOFER-INSTITUT FÜR MIKROELEKTRONISCHE SCHALTUNGEN UND SYSTEME IMS

ANNUAL REPORT 2012

ANNUAL REPORT OF THE FRAUNHOFER-INSTITUTE FOR MICROELECTRONIC CIRCUITS AND SYSTEMS IMS DUISBURG 2012

PREFACE

For Fraunhofer IMS the year 2012 was characterized by a fluctuating R&D revenue situation. The high level of the industrial revenues in 2011 couldn't be reached due to a weaker order situation of ASICs. With a constant number of employees in comparison to the previous year, the operating budget in 2012 amounted to 24 million euros – and thus it is at a similar level in comparison to 2011.

The successful cooperation with ELMOS in the area of CMOS processes as well as with Infineon in the area of SOI high voltage components could be continued and expanded in 2012.

The IMS business unit of uncooled infrared sensor technology on bolometrical basis has been enlarged and further industrial partners were acquired. The development of the bolometer processes could be pushed forward decisively with the result that these 25µ bolometers are expected to be finished in 2013. The Fraunhofer IMS with its activities in the area of uncooled infrared sensor technology intends to develop customized sensors for the automotive industry.

The business unit of wireless transponder systems acquired numerous new industrial partners in 2012 and also started many projects which will be finalized in 2013. The positive development of the industrial order situation in this area has contributed to the success of the institute in 2012.

In April 2012 the event "Smart X: Solutions for the future – What are the next steps for Smart Home, Smart Building and Smart City?" took place on the occasion of Klaus Scherer's farewell. Mister Scherer is the inventor and the "maker" of the Fraunhofer inHaus Center. Numerous renowned speakers discussed the prospective developments and challenges for our buildings and cities of the future. Mister Scherer was the head of the Fraunhofer inHaus Center until the end of 2012.

In June the Fraunhofer IMS CMOS Imaging Workshop took place in Duisburg for the sixth time – meanwhile an established forum of the European developers of image sensors. Under the slogan "EXTENDING THE DIMENSIONS" developers and experts in image sensors discussed the most recent trends in the industrial image processing for two days.

In October 2012 the division "Micro and Nano Systems" was founded under the direction of Prof. Dr. Michael Kraft. He moved from Southampton to the University of Duisburg-Essen where he has been offered the professorship of Integrated Micro-Nano Systems. The business unit "Pressure sensors" as well as the business unit "Biohybrid systems" belong to his department.

In the fourth quarter of 2012 the company NovioSense BV was founded in The Netherlands. A system for a bloodless and wireless measurement of the blood glucose level for diabetic patients will be developed. A biosensor of the Fraunhofer IMS which is located at the body of the patient will continuously measure the glucose level in other body fluids than blood like sweat or eye fluid. That's how the permanent blood sugar measurement with a peak in the finger can be omitted in future.

The authorization for our biohybrid laboratory has been granted in the beginning of 2012 and the construction work could start a little later. Equipment and instruments for the development of biosensor systems with a total value of approx. 500.000 euro were installed on 45 sqm.

To expand the topic area of high-temperature electronics in a continuously way a workshop on this topic was carried out at the Fraunhofer IMS. 16 national and international speakers and more than 100 developers and participants met each other at the two-day workshop, where our Fraunhofer SOI CMOS processes were one of the central topics. With these processes high-temperature circuits with operating temperatures up to 250 °C like e. g. EEPROMs can be realized. With a common Fraunhofer project (HOT300) the research within this area will be extended in the future. Operating temperatures up to 300 °C and their process engineering feasibility are in the focus of the R&D work.

The expansion of our CMOS assembly line and the test rooms for wafer series has been completed in the middle of 2012. Now the Fraunhofer IMS has equipment, facilities and rooms on 120 sqm which comply with the high-level requirements, also for the construction of image sensors. Here, a total of over 1 million euro was invested.

My special thanks go to our employees who have enabled the economic and scientific success in 2012 by their dedicated work. Despite the current uncertainties in the euro zone and the associated difficult market prospects we are well prepared for the future. I would like to thank all our business partners for the trustful and excellent cooperation in 2012. We look forward to the new and exciting tasks in 2013.

Anton Grabmaier

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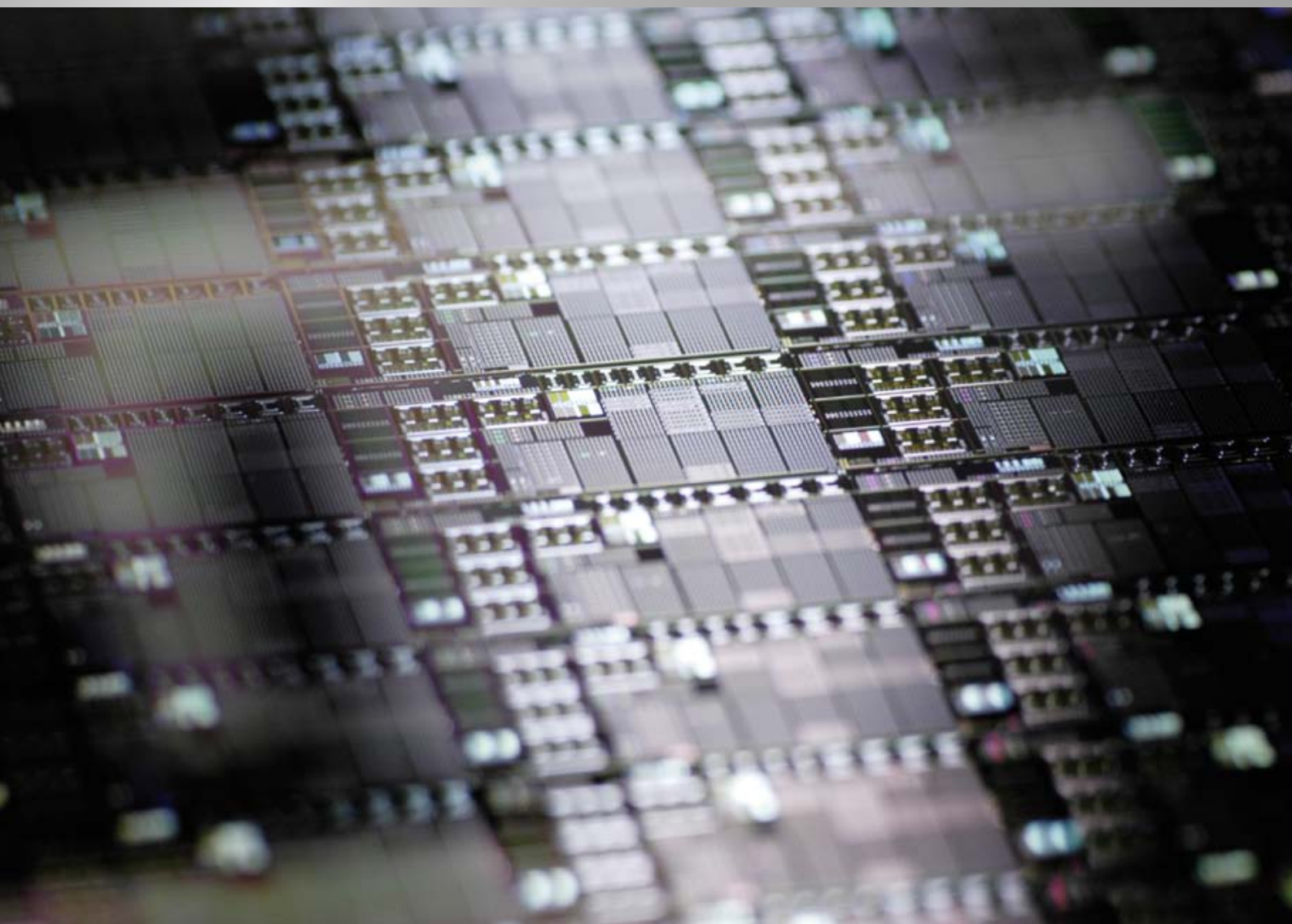
CONTENTS

PROFILE



YOUR IDEA – WE WILL IMPLEMENT IT

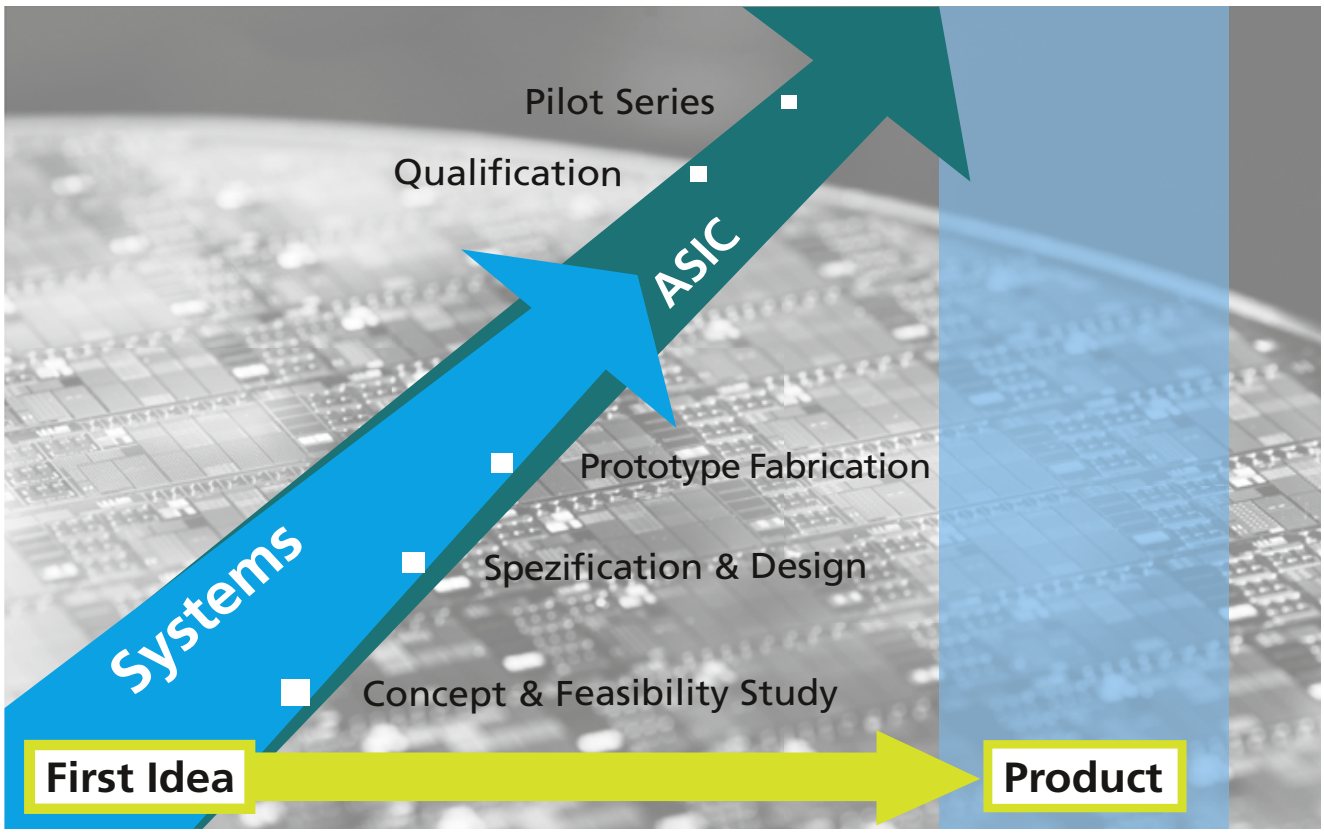
Your Product Idea

In the beginning there's your idea or vision for a new product, but you don't know if it is feasible, which costs you will have to face, if there are potential risks and which is the technology that leads to the optimal product. As a research and development institute of the Fraunhofer-Gesellschaft we offer you our support.

We accompany your development with concept and feasibility studies from the first moment – via specification and design, draft and fabrication of prototypes through to the product qualification.

The pilot fabrication of your circuits and ICs is carried out by us as well. With us, you get microelectronics from a single source.

We provide our service and know-how across all industries. Our circuits and systems are especially used where it's all about the creation of unique selling points and competitive advantages for our customers. Then, our customer is able to serve his target market in an optimal way.



Step by Step to Project Success

The way to a successful project is work-intensive and requires a good planning. Step by step, the following project phases are passed through:

- Concept & Feasibility Studies
- Specification & Design
- Demonstrator Development
- Prototype Development
- Qualification
- Pilot Fabrication (for ASICs)

Quality Pays off

The Fraunhofer IMS is certified according to DIN EN ISO 9001 since 1995. The certificate is valid for all divisions of the institute: Research, development, production and distribution of microelectronic circuits, electronic systems, microsystems and sensors as well as consulting in these fields. The CMOS line is certified according to ISO/TS 16949.

Your project success is our mission.

Our Business Units

- IC Design & ASICs
- Wireless Systems & Transponders
- Ambient Intelligence Systems
- Pressure Sensor Systems
- CMOS Image Sensors
- IR-Imagers
- Devices & Technology
- Biohybrid Systems

FROM WAFER TO SYSTEM

Our technological home at Fraunhofer IMS is, since the foundation in 1984, the semiconductor technology and the development of microelectronic circuits and systems. The type and bandwidth of our infrastructure is extremely efficient; we have the experience and know-how in eight business units.

During our contract works we focus on strong, efficient and marketable developments. We offer comprehensive technologies and procedures which are applied in almost all industries. Application-specific adaptions to the requirements of our customers are the major focus of our work.

Our Technological Core

- Semiconductor Processes
- CMOS & SOI-Technologies
- Microsystems Technology
- Component & System Developments
- Nano-(Bio)technologies

Infrastructure

CMOS Assembly Line

Wafer size	200 mm (8 inches, 0.35 µm)
Cleanroom area	1,300 m²
Cleanroom class	10
Employees	150 in 4 shifts
Capacity	> 70.000 wafer/year

Microsystems Technology Lab & Fab

Wafer size	200 mm (0.35 µm)
Cleanroom area	600 m²
Cleanroom class	10
Capacity	5.000 wafer/year

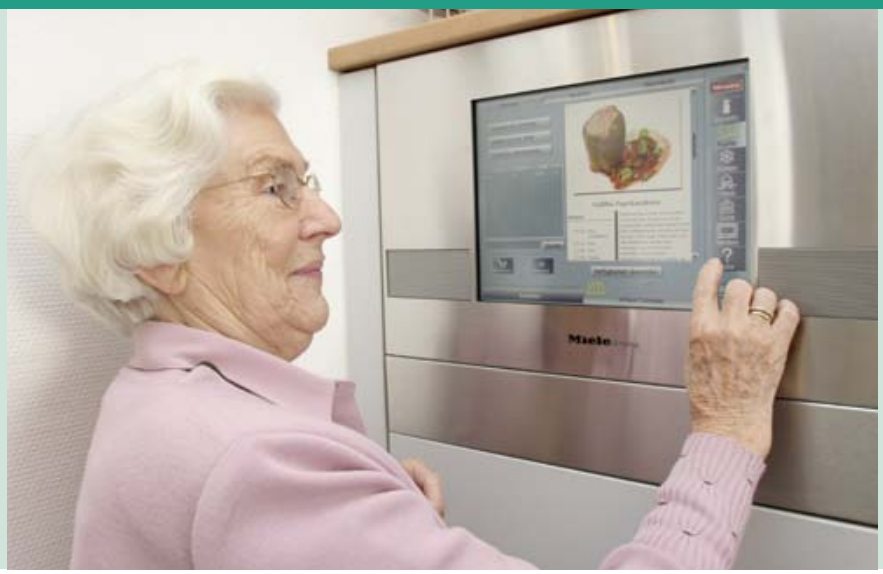
Cleanroom for Test & Assembly

Wafer size	200 mm
Cleanroom area	1.200 m²
Cleanroom class	1.000
Test	5 test systems
IC-Assembly	Sawing & thinning of wafer
	Chip-On-Board
	Die- and wire bonding

Laboratories

Biohybrid sensors	45 m²
inHaus center	3.500 m²
Laboratory space	800 m²
High-frequency Measurement Chamber	24 m²

AMBIENT INTELLIGENCE SYSTEMS



People spend a large part of their lives in rooms and buildings. Not only private living but also care processes – at home or in nursing homes – and the whole working life usually take place in buildings. Here, operating costs, a flexible adaption to user requirements and the feel-good factor are becoming increasingly important.

In our inHaus-center, supportive solutions for residential and building environment (AAL – Ambient Assisted Living) for our customers are developed and also tested. The installed products for facility management in commercial buildings are subject to criteria of high economic efficiency and sustainable energy efficiency.

The Fraunhofer IMS offers novel assistance systems for more efficiency in the nursing and hospital area. Innovative solutions in the area of energy & facility management up to solutions for the next generation office are the development priorities in the business unit Ambient Intelligence Systems.

We provide our service and know-how across all industries. Our circuits and systems are especially used where it's all about the creation of unique selling points and competitive advantages for our customers. Then, our customer is able to serve his target market in an optimal way.

Supply and Services / Technology

- Hard- and software development
- Planning and consulting
- Building integration and practical tests
- Heterogeneous interconnection (also wireless)
- Field tests for long-term monitoring

WIRELESS SYSTEMS & TRANSPONDERS

Industrial production and processing processes can only supply high quality products and work cost-effectively if the machines are optimally adjusted, if they haven't got much wear and possess a long durability. For the performance of these requirements it is indispensable to have measurement data which help to optimize the machine settings, to determine the maintenance requirements, to control the manufacturing steps and to make quality recordings.

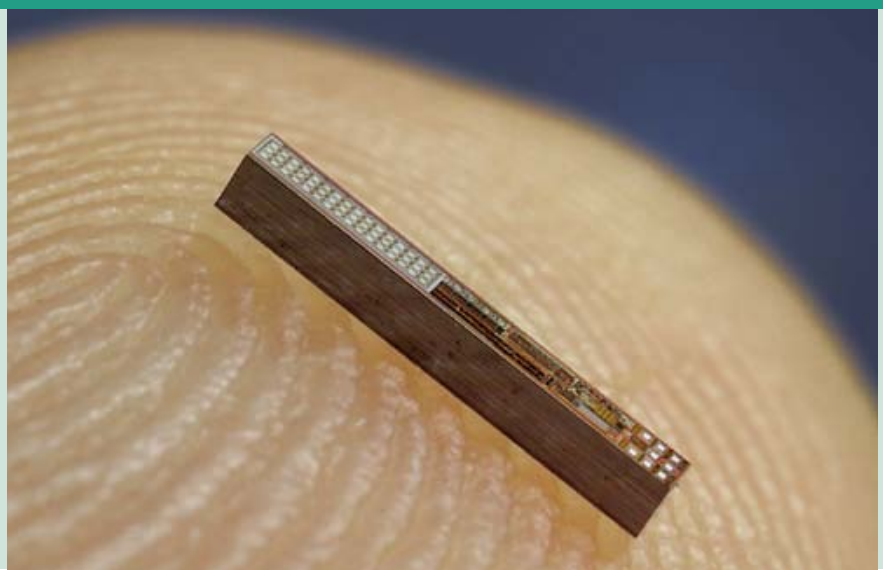
Transponder systems – especially sensor transponder systems – and sensor networks feature an excellent technological basis for the registration of identification and sensor data.

The wireless communication and power supply open up new application areas – e.g. in medicine to get measurement data from implanted sensors for diagnostic and therapeutic purposes. Other interesting application areas are the building sector and logistics.

Supply and Services / Technology

- Active and passive systems
- Sensor transponder integration
- Customized adaption
- Funk-frontends for LF-, HF- & UHF-frequencies
- Systems with high ranges
- Systems for "difficult" environments

PRESSURE SENSOR SYSTEMS



In microelectronics the trend is toward smaller and smaller sensors even in pressure sensor technology. Our customized developments are not only particularly efficient and consume little power but they are also, due to their minimal size, implantable in the human body if required. For this reason, beyond classic applications of pressure sensor technology, new fields of application are opened up, particularly in medical engineering.

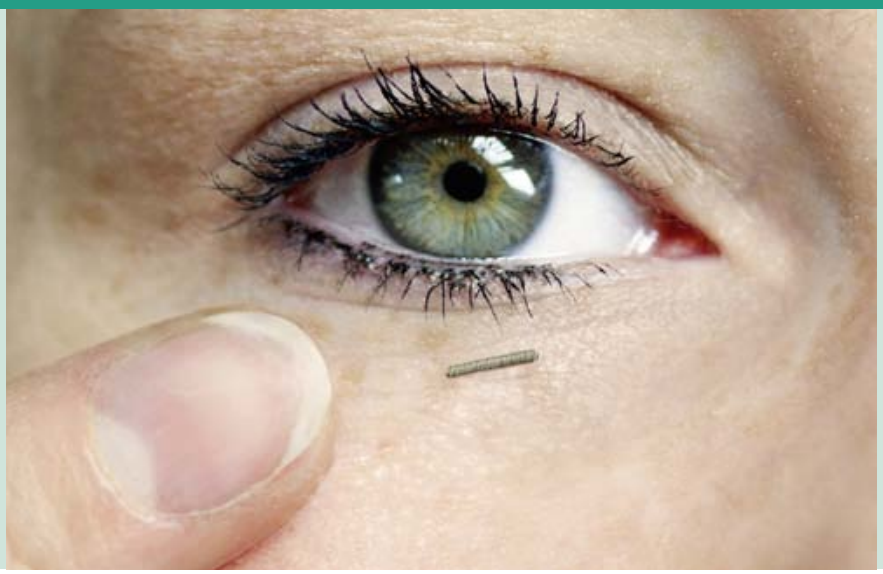
By the fabrication of these sensors as integrated capacitive pressure sensors in surface micromechanics a connection with any signal processing is possible.

Our miniaturized pressure transponders are also suitable for metrological applications in industry or for the measurement of tire pressures in automotive engineering. Due to the integration of the sensor system and signal processing in one ASIC the Fraunhofer IMS can cater to all realizable requirements and applications and can offer customized technologies for the future.

Supply and Services / Technology

- Customized development of capacitive pressure sensors
- Measurement range of just a few mbar up to 350 bar
- Extremely high precisions
- Transponder ability due to low energy requirements
- Integrated temperature sensor
- Customized packages, tests & calibration

BIOHYBRID SYSTEMS



The markerless identification of biological and chemical substances without extensive laboratory work is decisive for the progress in medical engineering. Sophisticated measuring technology is replaced by miniaturized systems which recognize substances via a biosensor (immuno or electrochemical sensor) by their electronic reaction.

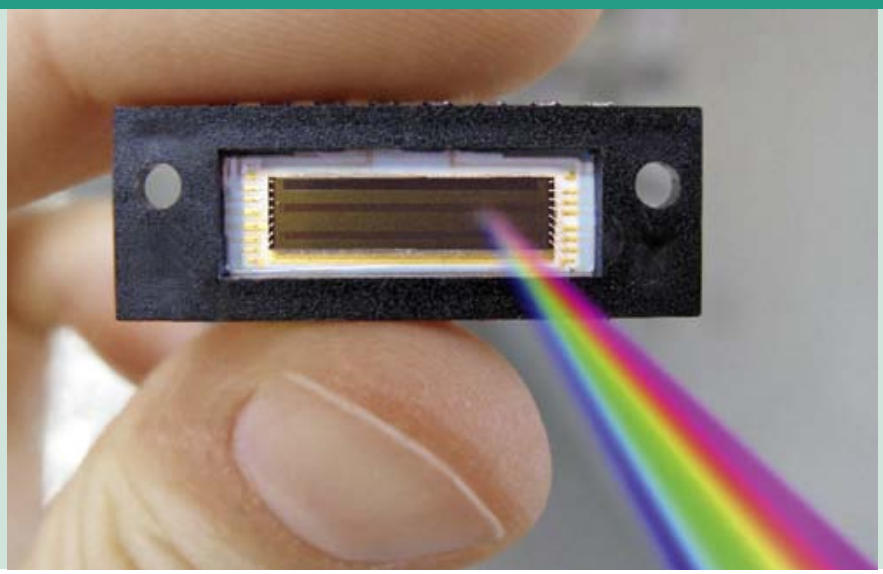
We offer the development of these highly sensitive detection systems, which state a cost-effective and fast option to optical analyses in the laboratory. These nano systems can also be integrated into more complex biohybrid systems, such as Lab-on-chip, if required. This is particularly interesting for customers of medical engineering, who can offer simple ways for real-time examinations via non-invasive, permanent diagnosis and monitoring systems in the future.

Because bioelectronic sensors can detect medical and physical parameters. These functions are also interesting for the food industry, which can profit by the simple and fast detection of biological-chemical variations of their products.

Supply and Services / Technology

- Customized biosensor systems (e.g. glucose, lactose)
- Markerless and quantitative sensor technology
- Real-time monitoring in body fluid
- Customized electrochemical sensor technology
- Customized immuno sensor technology
- Customized packages and tests

CMOS IMAGE SENSORS



Sensors for image capture based on CMOS technologies have reached a point where its quality and performance even surpasses the outmost mature CCD sensors. Development of special photo detector devices or the special treatments of the silicon surface boost the pixel attributes. Our long experience in designing CMOS photo detectors and imagers, as well as their processing and characterization enable custom solutions that meet customers' requirements.

Our customers profit from a 0.35 µm "Opto" CMOS process optimized for photo sensing applications. »Pinned« photodiodes with low dark current and noise with color filters, micro lenses and also stitching can be integrated.

Our developments cover a wide spectrum from roentgen-rays to EUV, UV and the visible area up to the near infrared-range.

Supply and Services / Technology

- Customized line and area sensors
- Special pixels for time-of-flight, spectroscopy et al.
- Stitching for large-area sensors
- UV- and XUV-sensitive sensors
- Color filters and micro lenses
- Customized packages and tests
- Pilot fabrication in the 0.35 µm "Opto" CMOS proces

IR SENSORS

Infrared imagers »see« in a wave length range from the near up to the long-wave infrared. These thermal image sensors are called focal plane arrays and are one- or two-dimensional lines of IR-sensitive pixels. They are based on radiation-sensitive structures on silicon technology, where CMOS read-out circuits are integrated on a chip. That's how complete image sensor chips are developed.

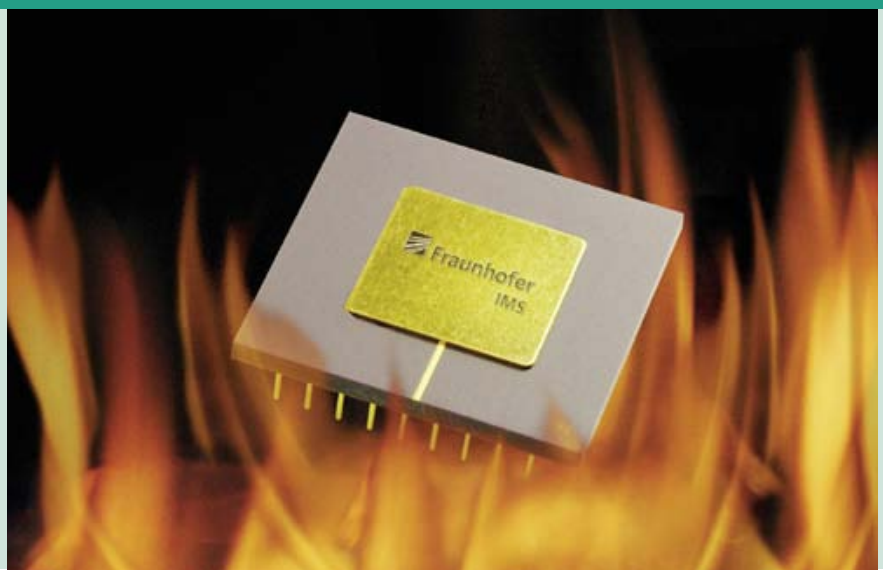
Our customer-specific applications are used in the automotive industry, where driver assistance, night vision and pedestrian detection are focal points of development.

In the industrial sector similar safety aspects, e.g. personal security, and also the measurement technology in the process monitoring matter. In the sensor system, the gas analysis is of increasing interest. Further applications are thermography in buildings or in medicine, but also for border and building security.

Supply and Services / Technology

- Customized IR imagers
- Complete on-chip signal processing
- Budget chip-scale packages
- IR development and pilot fabrication
- Customized packages, tests & calibration

IC DESIGN & ASICS



"From the concept up to the pilot fabrication" is the maxim of the Fraunhofer IMS. We provide our customers professional analogue or mixed signal ASIC design solutions – from the concept up to verified silicon for "ready to use" ASIC products for the application in several areas. In doing so, we support our customers with our large system know-how.

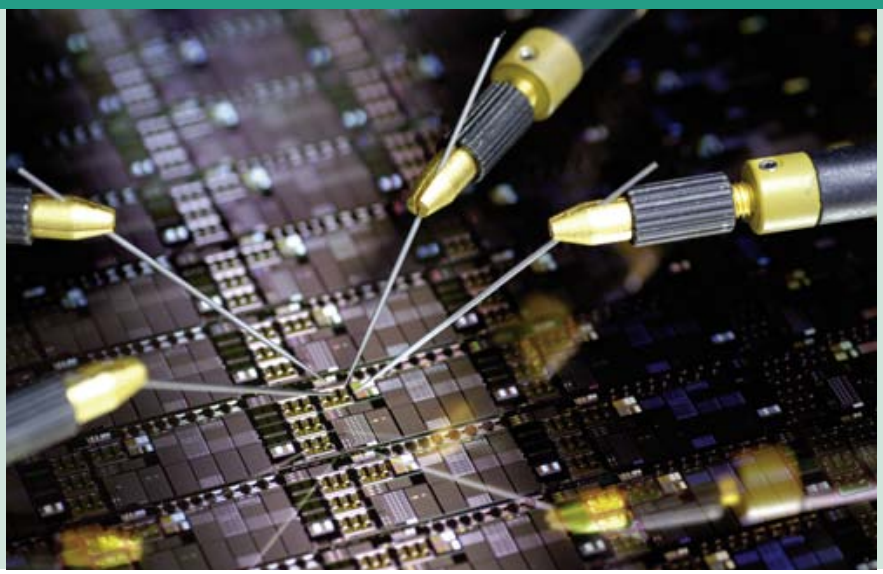
In addition to implementations in various standard CMOS technologies we especially allocate design and technology solutions for high temperature, high voltage and sensor systems applications.

Special circuit parts or sensor system components are individually and custom-designed developed and integrated with standard components like sensor readout, signal processing, interface components or embedded micro controllers on an IC.

Supply and Services / Technology

- Sensor interfaces
- Analogue ICs
- Signal conversion
- Digital signal processing
- Integrated sensors
- Customized packages and tests
- Energy-optimized solutions
- Pilot fabrication

DEVICES & TECHNOLOGY



Our in-house CMOS line is the technological base of our institute. It supplies professionally operated and acknowledged automobile quality in robust 0.35 µm technology on 200 mm wafer. The entire processes are developed in the Fraunhofer IMS and are extended by additional process modules, such as special optical devices, pressure sensors or high voltage components.

The integration of new materials or micromechanical structures is not possible by implication because a CMOS line has to be restricted to maintain the high level quality. Therefore, we have additionally assembled an own microsystems technology line (MST-Lab & Fab) for "post-processing".

CMOS wafers act as an "intelligent" substrate. They contain trigger and read-out circuits, signal processing and conversion as well as external interfaces up to the wireless power and data transmission. On these wafers, these "substrates", layers and structures are now deposited and by this new components are produced. The development's aim is to produce compact "intelligent" microsystems.

Supply and Services / Technology

- MST process developments
- Integrated microsystems on CMOS
- Wafer size 200 mm (0.35 µm)
- CMOS process development & devices
- SOI processes
- Development and consulting for the semiconductor industry

DIRECTIONS & CONTACT

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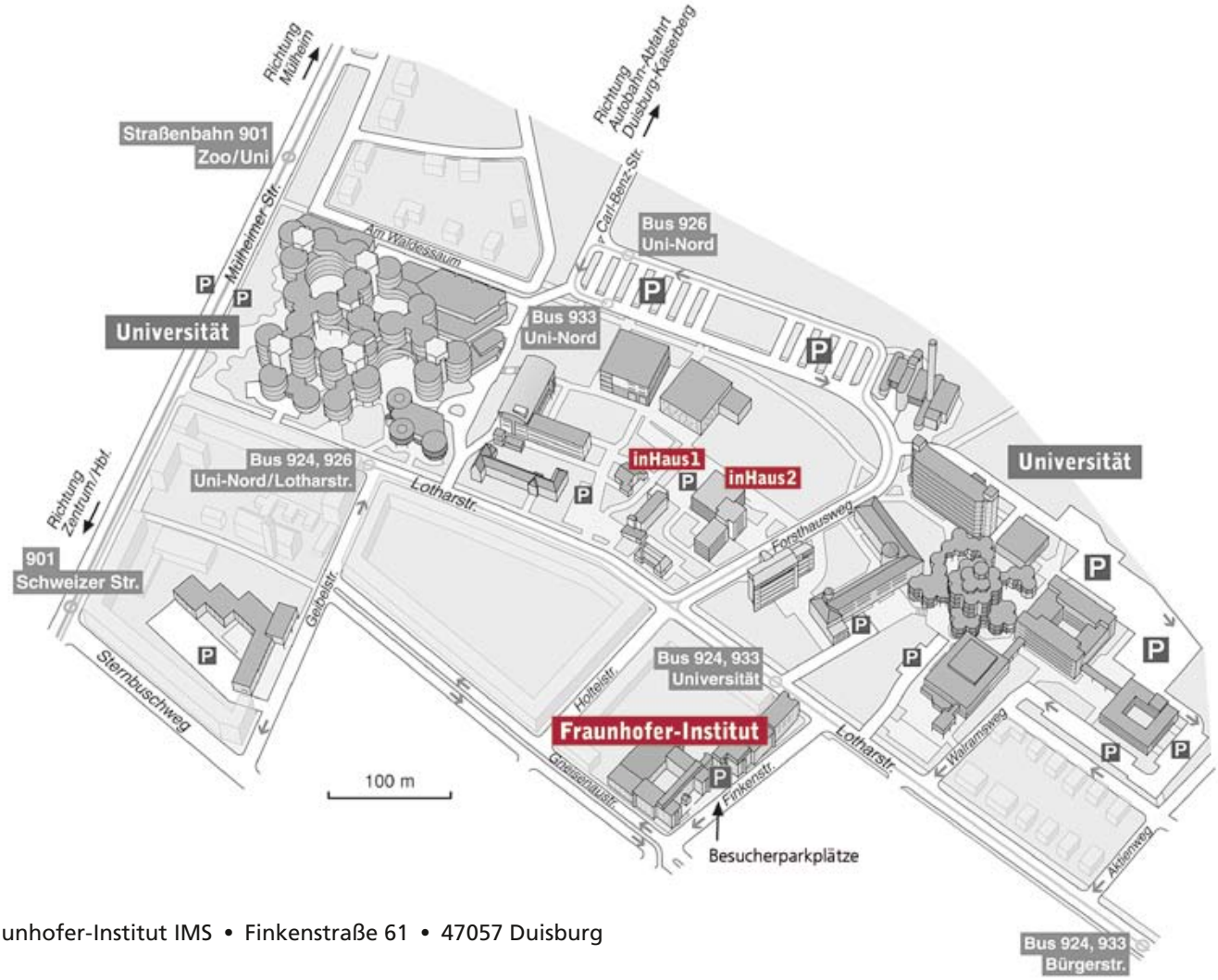
Access by car

via motorway A40

- exit "Duisburg-Kaiserberg"
- direction "Innenstadt", "Zoo"
- (Carl-Benz-Straße)
- after approx. 1 km (direction "Innenstadt") turn right into Mülheimer Str.
- pass the Zoo
- at first traffic light turn left into the Lotharstr.
- at third street turn right into Finkenstr.
- Institute is on the right side

via motorway A3

- exit "Duisburg-Wedau"
- direction "Innenstadt" (Koloniestraße)
- at traffic light turn right into Mozartstraße, which turns into Lotharstr. in the following of the street
- after 800 m turn left into Finkenstr.
- Institute is on the right side



Fraunhofer-Institut IMS • Finkenstraße 61 • 47057 Duisburg

Access by airplane

Arrival at Airport Düsseldorf

a) Taxi (duration 20 minutes)
b) to Duisburg Central Station by train from Duisburg Central Station take bus number 933 or 924 (direction Uni/Zoo), bus stop Universität

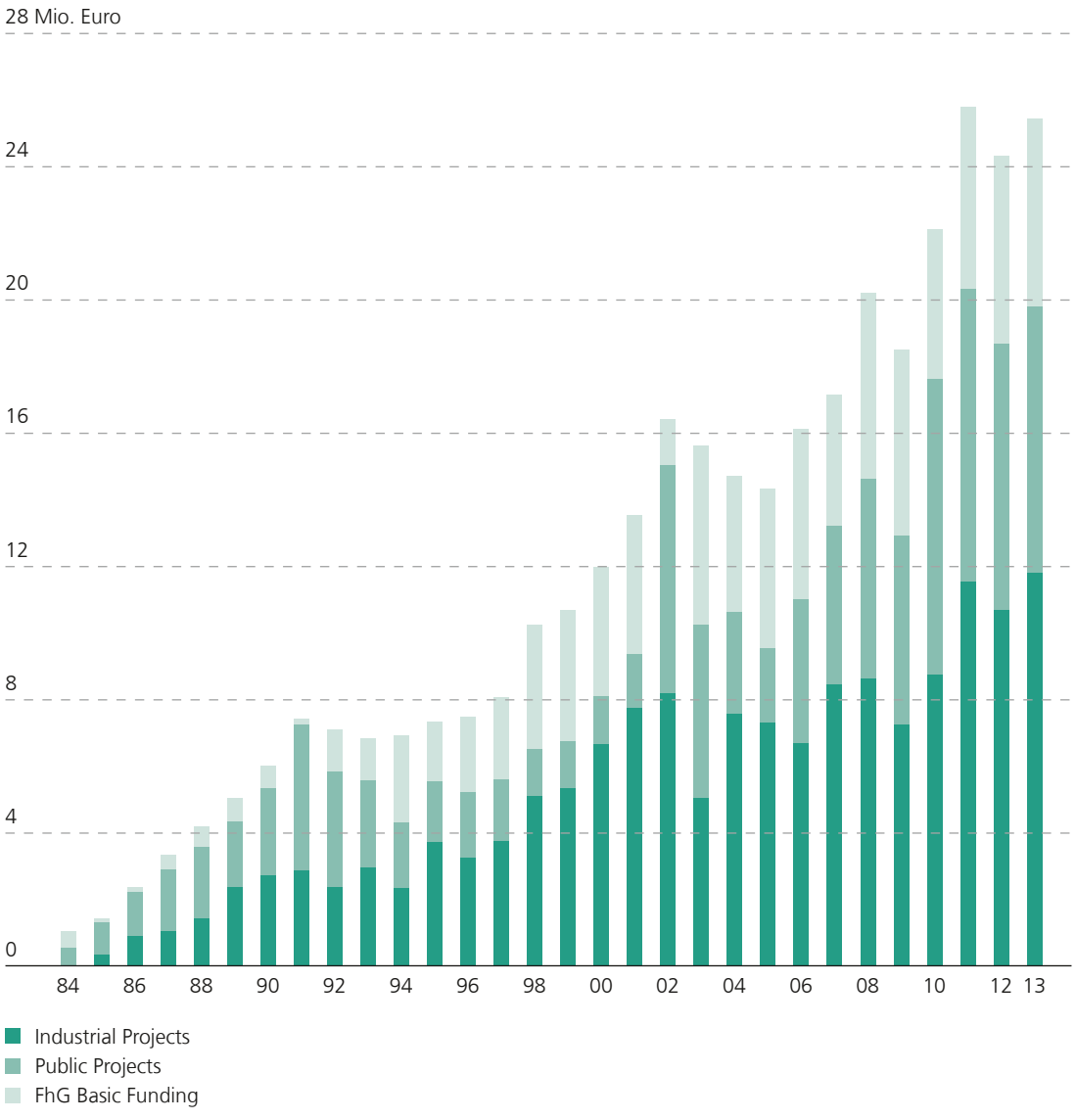
Access by train

Arrival Duisburg Central Station

a) Taxi (duration 5 minutes)
b) Bus line 933 or 924 (direction Uni/Zoo), bus stop Universität

DEVELOPMENT OF THE IMS

Budget IMS


28 Mio. Euro
24
20
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12
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84
86
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06
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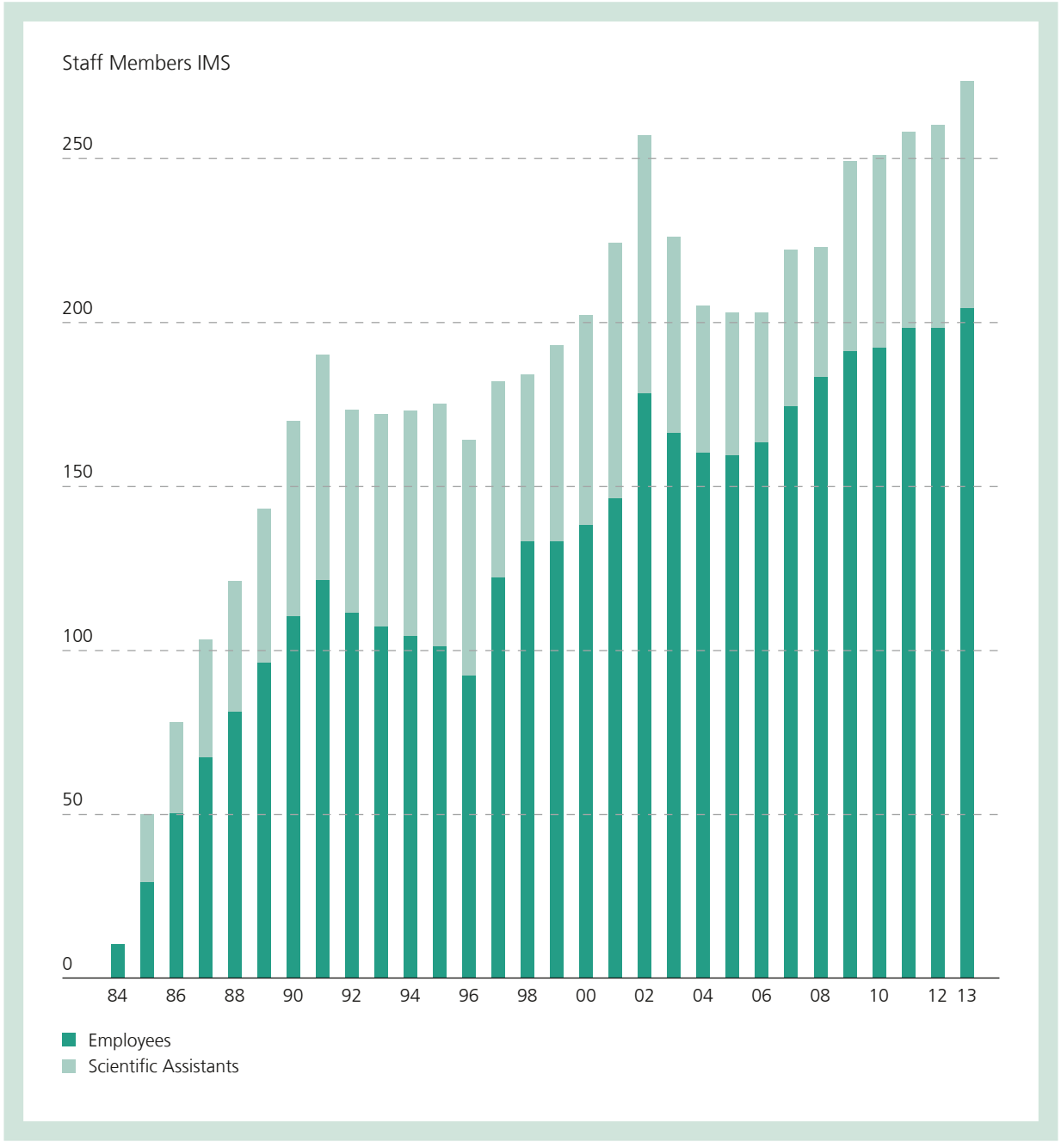
Industrial Projects
Public Projects
FhG Basic Funding


Staff Members IMS
250
200
150
100
50
0
84
86
88
90
92
94
96
98
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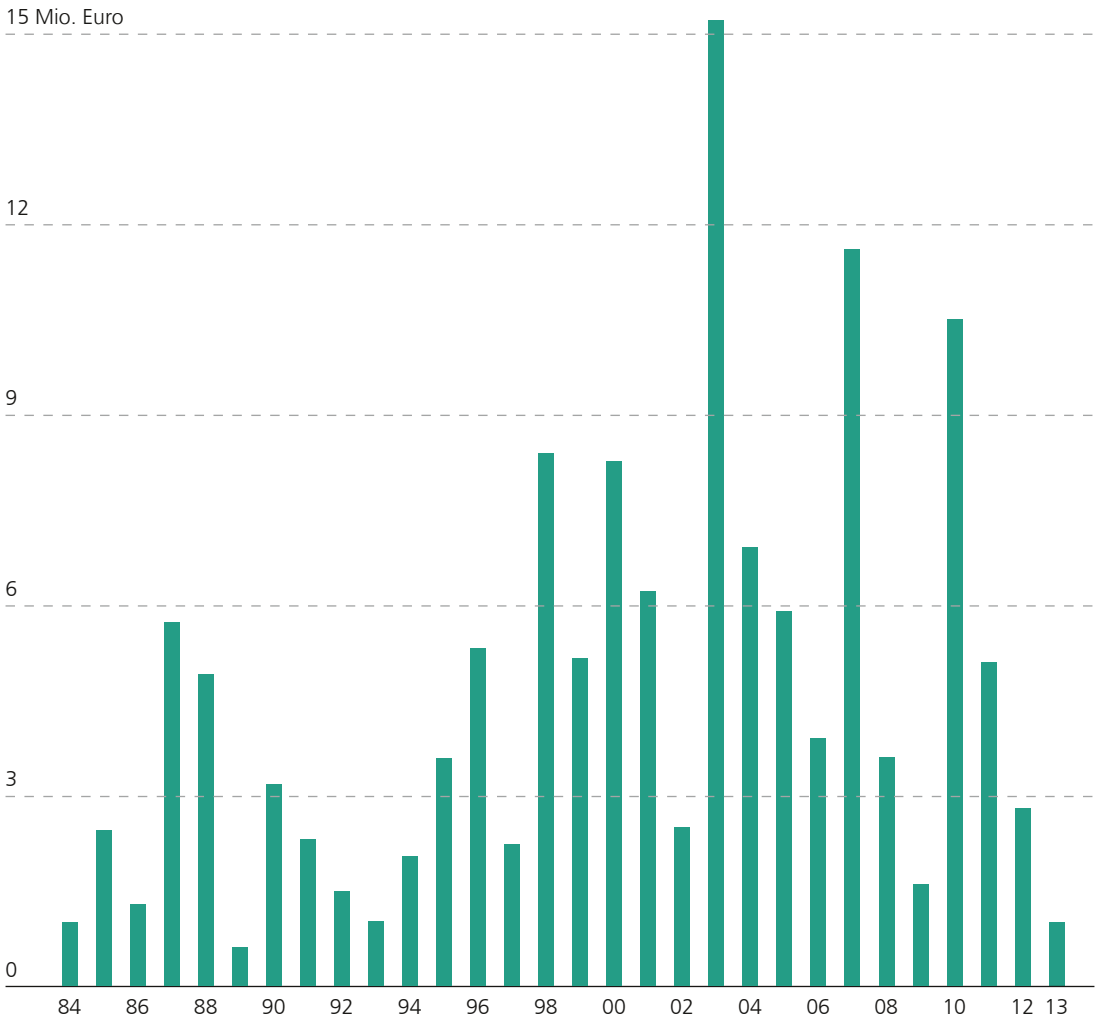
02
04
06
08
10
12
13
Employees
Scientific Assistants

Capital Investments IMS



SELECTED PROJECTS OF THE YEAR 2012

Selected Projects of the Year 2012

OPTICAL SIMULATION OF PHOTODIODES AND PHOTOCELLS MADE OF AMORPHOUS SILICON/GERMANIUM

A. Goehlich

1. Introduction

A wide class of optical devices such as photodiodes or photovoltaic (PV) cells rely on stacks of thin optically active films, i.e. films that convert absorbed photons into electrical charges. Basically in those devices electron-hole pairs (ehp's) are generated by light absorption. The ehp's are separated in the internal electric field generated by the outer electrodes and are transported by some mechanism (e.g. by drift or diffusion) to their respective collection electrode. A simplified energy diagram of such kind of photonic device is depicted in **Figure 1**.

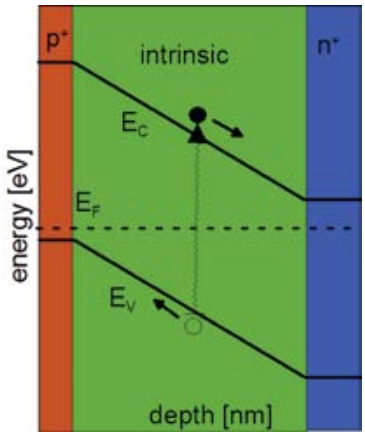


Figure 1: Schematic presentation of a p-i-n diode structure (without external bias)

For photovoltaic applications additional optical layers e.g. an anti reflecting coating (ARC), a transparent electrically conducting oxide (TCO) layer as an electrode and a back reflecting mirror are utilized. In particular CMOS compatible films made of amorphous silicon, amorphous germanium or silicon-germanium alloys are well suited to realize monolithic integrated optical elements like photocells or photo diodes in connection with an integrated driving or read out circuitry [1] because such films can be deposited at low temperatures < 450 °C by PECVD methods.

Amorphous silicon exhibits a wide optical band gap of about 1.7 eV, the band gap of bulk germanium is considerably smaller and amounts to about 0.66 eV enabling red and NIR extension of a-Si technologies. Therefore "band gap tailoring" has been performed by alloying a-Si layers with germanium [2] e.g. for stacked PV cells.

For the understanding and the optimization of such one dimensional layer stack devices a simple and fast optical modelling is required. For realistic simulations measured optical data for the complex refractive index $n(\lambda) = n_{re}(\lambda) + i\, n_{im}(\lambda)$ should be included. However also a lot of open sources for optical data [3], [4] are available.

Important quantities to be modelled are the local absorption of the light within the individual layers e.g. for p-i-n structures the absorption profile within the intrinsic layer and the resulting optical generation profile.

2. Calculational Method

In the course of customized development projects software has been developed that enables the calculation of the angular dependent reflection, absorption and transmission coefficients, but also of the internal electric fields, the energy fluxes and the absorption distribution within the layer stack are calculated. In particular the developed tool allows for the inclusion of in line measured data of the refractive indices.

A well known simulation technique for 1-d optical interference problems of multiple layers is the so called transfer matrix method. It is described in detail in several textbooks e.g. in ref. [5], therefore only a short summary is presented here. The method is based on the continuity of the tangential component of the electrical and magnetic field of a plane electromagnetic wave at the interface between adjacent materials. The simplest geometrical case is the perpendicular incidence of the light. A complex valued 2 x 2 matrix couples the electrical and magnetic field amplitudes (u_i, v_i) and (u_{i+1}, v_{i+1}) entering and exiting each layer of thickness d_i:

$$\begin{bmatrix} u_i \\ v_i \end{bmatrix} = \begin{bmatrix} \cos\delta_i & -i/n_i \sin\delta_i \\ -in_i \sin\delta_i & \cos\delta_i \end{bmatrix} \begin{bmatrix} u_{i+1} \\ v_{i+1} \end{bmatrix}$$

$$with\ \ the\ \ phase shift\ \ \delta_i = \frac{2\pi}{\lambda} n_i d_i$$

These matrices are multiplied for each layer to obtain the overall system matrix. The complex valued reflection and transmission amplitudes as well as the real valued intensity related reflectance and transmission coefficients are obtained from the elements of the system matrix by formulas e. g. presented in [5].

The case of perpendicular incidence can be easily extended to the oblique incidence case by substituting the refractive indices and the field amplitudes by angular dependent effective ones. In this case different matrix coefficients are obtained for the different polarizations of the light:

$$n_i \rightarrow n_i \cos\theta_i \quad for\ TE\ \ polarization$$
$$n_i \rightarrow n_i / \cos\theta_i \quad for\ TM\ \ polarization$$

The same substitution holds also for the effective field amplitudes. The angles θ_i, θ_{i+1} of the propagation vectors (with respect to the normal) between two neighbouring layers are coupled by the Snellius refraction law.

The field at each interface has been calculated iteratively starting with the amplitude of the transmitted field at the exit layer (calculated with the aid the previously determined transmission amplitude coefficient) and multiplying with the corresponding last transfer matrix.

The fields ($u_i(z)$, $v_i(z)$) inside each layer are decomposed in a forward and a backward running wave, whose amplitudes are determined with the aid of the previously calculated interface fields at the entrance and exit interface of each layer. The spatially resolved energy flux (i.e. the Poynting vector S(z)) and the differential absorption (i.e. the negative spatial derivative of the energy flux dS/dz) inside each layer is then easily obtained from the electrical and magnetic fields.

3. Optical simulations of photo cells

An important parameter in the characterization of photonic devices is the efficiency. For broad band illumination with an illumination spectrum I_λ (λ) a simple figure of merit (FOM) to be maximized can be derived from the short circuit current J_{SC}:

$$FOM \propto J_{sc} = \frac{e}{hc} \int_{\lambda_1}^{\lambda_2} d\lambda\ \lambda \sum_j a_j(\lambda)\, \eta_{\text{int}}^{(j)}(\lambda) \quad I_\lambda(\lambda)$$

Here $a_j(\lambda)$ denotes the absorption within *the optically active* layer j and $\eta^{(j)}_{\text{int}}$ is the internal conversion efficiency that accounts for the conversion of an absorbed photon to a electronic charge reaching the collection electrodes. In the ideal case the value of η_{int} approaches unity. Due to the short recombination length in the highly doped layers only the intrinsic layers are considered in the calculation of the FOM for amorphous p-i-n-diodes. The integral extends over the sensitive spectral interval of the optical device, typically limited by the cut off due to the transmission of the optics and the band gap of active material.

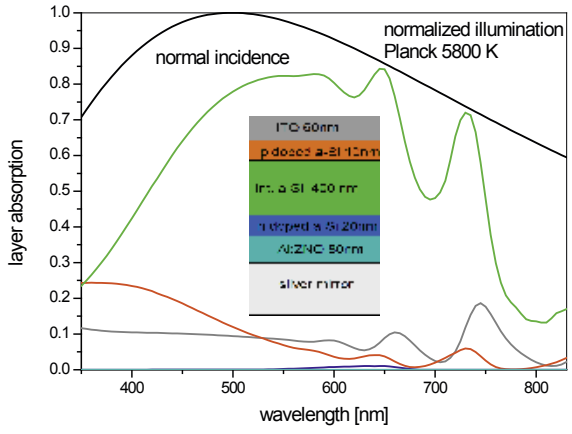


Figure 2: Spectrally resolved absorption of a single PV cell (Absorption of intrinsic layer in green)

OPTICAL SIMULATION OF PHOTODIODES AND PHOTOCELLS MADE OF AMORPHOUS SILICON/ GERMANIUM

As application examples the spectrally resolved layer absorptions for an a-Si single and an a-Si/SiGe tandem PV cell are depicted in the **Figures 2 and 3** together with the assumed layer stack.

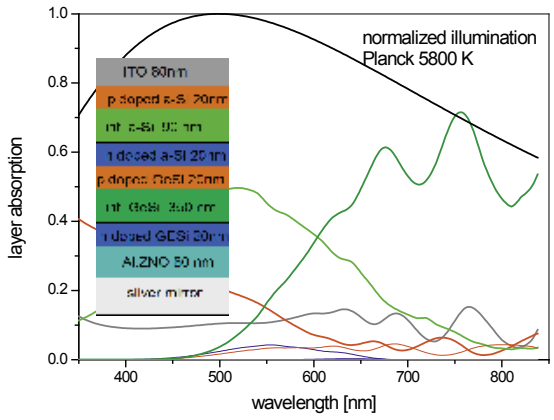


Figure 3: Spectrally resolved absorption of a tandem cell

Perpendicular incidence and an illumination with a normalized Planck-spectrum approximating an AM 1.5 sun illumination have been assumed for calculation of the FOM. In order to optimize the efficiency the FOM has been calculated for several thicknesses of the ITO layer. It exhibits a distinct maximum for a thickness of about 60 nm. For the tandem cell a series arrangement of two p-i-n diodes with an a-Si and a GeSi active layer has been assumed. It is observed for the tandem cell that the infrared response is significantly increased by the GeSi layer (**Figure 3**). The spectral data have been taken from refs. [3], [4]. The calculated internal energy flux and the differential absorption of the single cell are depicted for different wavelength in **Figures 4 and 5**.

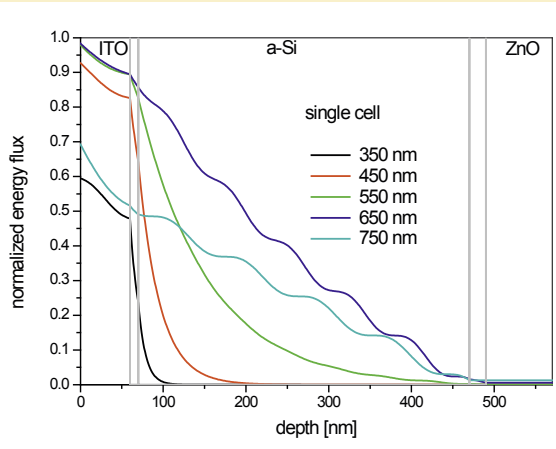


Figure 4: Normalized energy flux for different wavelength

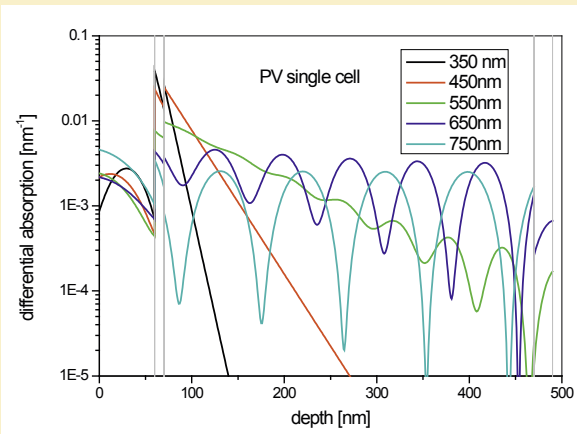


Figure 5: Differential absorption for different wavelength (single cell)

It is observed that the shape of the differential absorption changes from an exponential behaviour at the blue side (i.e. strong absorption) to a shape with a superposed oscillation (due to multiple reflections) on the red side (i.e. low absorption) side of the spectrum. While the energy flux is continuous at the interfaces, the differential absorption exhibits discontinuities caused by the different refractive indices.

The differential absorption can be transformed into an optical generation rate by the relation:

$$G_{opt}(z) = -1/hc \int_{\lambda_1}^{\lambda_2} d\lambda \, \lambda \, I_\lambda(\lambda) \frac{dS}{dz}(\lambda)$$

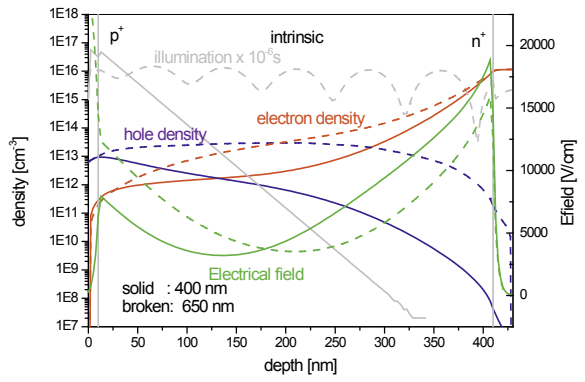


Figure 6: Calculated distributions with monochromatic illumination (400 nm and 650 nm) through p⁺ layer

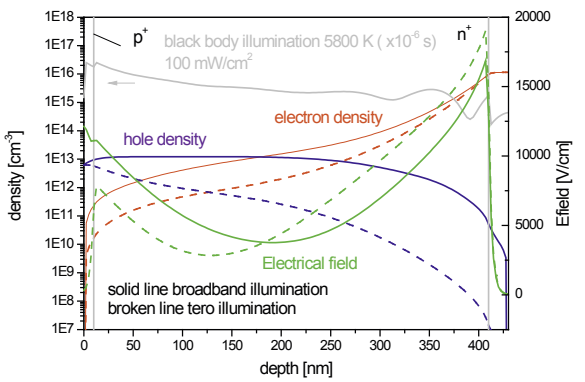


Figure 7: Calculated distributions with Planck illumination through the p⁺ layer (at 0.75 V forward bias)

The calculated generation rate can be coupled to a device simulation. In the following example a 1 d-calculation of the amorphous a-Si p-i-n-structure (see Fig. 2) performed with the device simulator DESSIS is presented. Trap recombination within the amorphous silicon layers has been described by two exponential band gap tails and two near mid gap Gaussian distributions for acceptor and donor states respectively [6]. The band gap has been assumed to 1.7 eV. The mobility of the carriers is considerably reduced as compared to the value in crystalline silicon: values of $\mu_n = 10\ cm^2/Vs$ and $\mu_p = 1\ cm^2/Vs$ were assumed. The distribution of the carrier densities and the electric field is depicted in **Figure 6** for blue (400 nm) and red (650 nm) monochromatic illumination at 0.75 V forward bias (near MPP) of the diode. An intensity of 100 mW/ cm² has been assumed for the illumination in each case. It is observed that the "red" generation profile penetrates deeply in the material enhancing the electron and hole densities near their collection electrodes leading to higher efficiency. The minimum of the electrical field is shifted to the n⁺-electrode. Similar findings are reported in ref. [7].

Figure 7 shows the result for the illumination with a broad band black body spectrum (5800 K) in the spectral range 350 – 830 nm as compared to zero illumination case.

The resulting generation profile extends deeply in the material and substantially enhances the density of the holes.

The device simulation allows also to estimate the internal conversion factor hint for this example. Values near unity are found with only weak wavelength dependence justifying the calculation of the FOM with $\eta_{int} = 1$ as a first approximation see **Figure 8**.

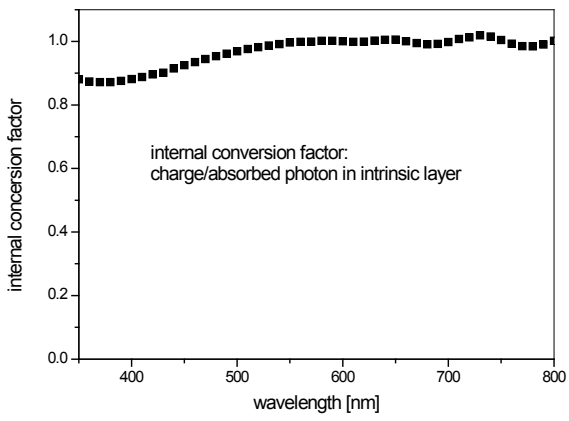


Figure 8: Calculated internal conversion factor

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DEVELOPMENT OF HIGH VOLTAGE FOR A 0.18 µm CMOS PROCESS: A HETEROGENEOUS TECHNOLOGY ALLIANCE PROJECT

S. Dreiner, S. Weyers, M. Mehta, U. Paschen

In this project the competences of the Heterogeneous Technology Alliance (HTA, an alliance of four major European research institutes: CEA LETI, CSEM, VTT and Fraunhofer) in silicon technologies were combined to support Altis semiconductor in the development of a new CMOS High Voltage process with 0.18 µm design rules. CEA LETI and FhG IMS together provided ALTIS with R&D support to develop HV MOS transistors, bipolar transistors, Zener and Schottky diodes. FhG IMS and CEA Leti joined their expertise in modeling, parameter extraction, simulation and process development for this new high voltage devices process in the Altis clean rooms.

TCAD desk and device optimization

At the beginning of the project the wafer material was defined (especially epitaxial layer doping and thickness). The epitaxial layer process was developed by LETI. A TCAD setup for the new technology to enable process and device simulation as a basis for the device optimization was developed by IMS. The process flow was translated into Synopsys Sentaurus Process code. Also layer thicknesses, STI shape and doping profiles of the simulation were calibrated with the real world results. The meshing and calculation time had to be optimized. And last but not least the simulations for different device parameters had to be carried out in order to understand and optimize the device characteristics.

Figure 1 shows some process simulation results for a high voltage MOS transistor. The high voltage transistor uses a lateral drift region (region II) to achieve higher maximum drain voltage (target 24V). For these devices simulations with varied drain extension length (region II), channel length (region I) and doping profiles were carried out in order to optimize transistor for the 24 V voltage range.

High Voltage MOS model and parameter extraction

A main task in the project was the development of the parameter extraction procedure for the high voltage transistors. For high-voltage transistors there are a few commercial compact models (HiSIM HV, Phillips MM20 , HV EKV …) available. Another approach that is followed by many companies (including IMS), due to the lack of a good compact model in the past, is the use of a BSIM3 based macro-model. BSIM3 does not include specific high-voltage effects, such as drain extension, quasi-saturation and self-heating. In order to account for these effects, they were implemented in a sub-circuit extension (macro-model) (cf. Fig. 2).

The convergence behavior depends on the complexity of the sub-circuit. If only a few additional parameters are used a good convergence can be observed with the disadvantage of a less perfect device characteristic (not all effects are included). LETI and IMS decided to start with a macro model instead of more complex compact model for the high voltage transistor parameter extraction.

The IMS proposed a macro model [1] that is displayed in Fig. 1. To model the effect of the drain extension the HV transistor is

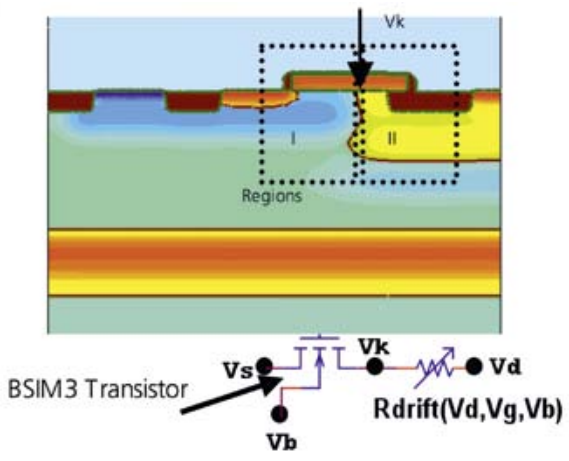

Figure 1: TCAD simulation results for a high voltage transistor. A BSIM3 based macro-model is used for circuit simulations. The transistor is split into an intrinsic BSIM3 transistor (Region I) and a bias dependent resistor (Region II).

DEVELOPMENT OF HIGH VOLTAGE FOR A 0.18 µM CMOS PROCESS: A HETEROGENEOUS TECHNOLOGY ALLIANCE PROJECT

divided into an intrinsic MOSFET region (region I) and a drift region (region II) in the drain extension. The intrinsic transistor region was thereby represented by the standard BSIM3 model and the drift region by an additional bias dependent resistor.

For proper modeling of the drift resistor at first the effects of gate induced charge accumulation (parameter: PHIACC) should be considered. Increasing the gate voltage induces accumulation carriers in the drift region and thus lowers its resistance.

Also the effect of body voltage induced depletion (PRWB2) should be included. The applied body voltage increases the depletion zone of the low doped drain extension resistor and thus increases the R_{drift} resistance (cf. Fig. 2 region 1):

$$R_{drift0} = \frac{R_0 * \left(1 + PRWB2 * |V_{bs}|\right)}{1 + PHIACC * |V_{gs}|} * \frac{1}{W + dW}$$

The model should be able to effectively describe the observed delayed transition between linear and saturation regimes and the quasi-saturation effect at high gate voltages (cf. Fig. 2 region 2). This effect occurs due to carrier velocity saturation in the drift region and is equivalent to an increase in the drift region's resistance. It can be modeled by making the drift resistance directly dependent on the electric field applied to the drift region:

$$R_{drift} = R_{drift0} * \left[1 + \sqrt{\left(\frac{V_d - V_k}{VSAT}\right)^{asat}}\right]$$

Where V_d-V_k is the voltage drop across the drift resistor and VSAT and asat are the velocity saturation parameters.
The self-heating effect (SHE) occurs because the high power dissipated in the high-voltage MOSFET increases the internal device temperature T. Due to the temperature increase the resistance increases for high voltages and currents (cf. Fig. 2 region 3).

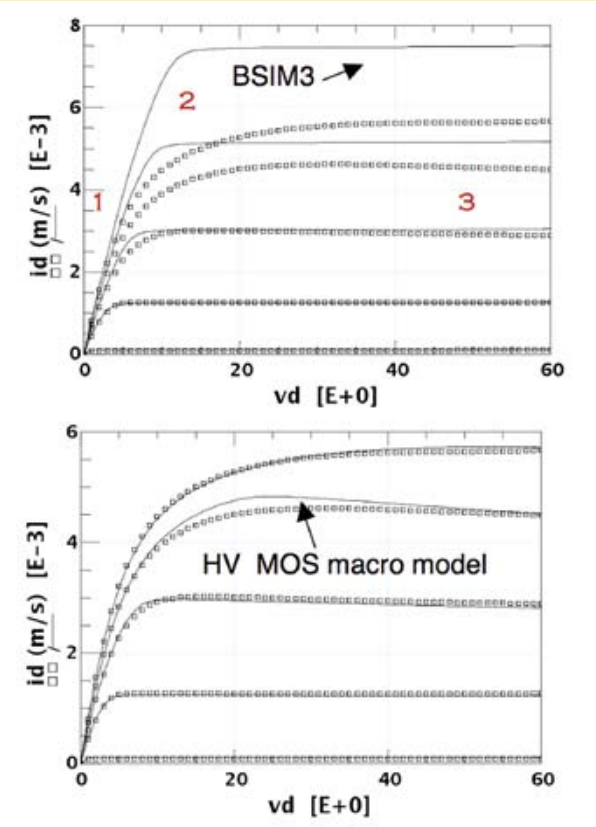

Figure 2: Output characteristic of a high voltage transistor (symbols display measurements): top: comparison with standard BSIM3 model without high voltage effects (lines); bottom: comparison with BSIM3 based high voltage macro model (lines).

The SHE is described by a standard thermal sub-circuit that includes a thermal resistance R_t and a thermal capacitor C_t. The power dissipation Pd of the transistor is injected into the sub-circuit as the current with value $V_d * I_d$, leading to the voltage drop across the resistance R_t and capacitance C_t. This voltage drop is proportional to Pd and represents the internal device heating rate ΔT.

For the extraction and optimization of model parameters the Agilent ICCAP program was used. BSIM3 and sub-circuit

model parameters from HV NMOS transistors were derived in a sequence developed by Fraunhofer IMS. The sequence is a mixture of pre-defined BSIM3 extraction routines and new routines especially added for the macro model.

This extraction procedure was tested by IMS on the TCAD simulation results for the high voltage transistors. 12V/24V HV MOS parameter extractions on silicon were performed successfully by LETI based on by IMS developed parameter extraction sequence and macro model.

Parameter extractions for the new bipolar transistors and standard MOS transistors (LETI) using standard models were also performed by IMS (Bipolar) and LETI (MOS). Further investigation by IMS on process and device development for the 48V/60V range based on TCAD and a literature survey show ALTIS how to proceed with technology development for this interesting voltage range.

Conclusion

The project is an example for the synergy effects of the cooperation within the HTA to support European industrial partners. In the project new devices especially high voltage transistors were developed and integrated which enabled Altis to address new application fields and to benefit from the different know-how of the involved institutes.

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THE BIOHYBRID LABORATORY FACILITY

T. Zimmermann, M. Kraft, S. Pierrat

Introduction

Biohybrid system technology is an emerging interdisciplinary R&D field at the interface of nanotechnology, material science, biotechnology, biophysics and electronics. There is little doubt that biotechnology will be a key technology for the 21st century with tremendous potential to address pressing societal needs but also for commercial exploitation. In the context of microelectronics and microelectromechanical systems (MEMS) applications, the goal of biohybrid system technology is mainly guided by the design and implementation of customized biosystems incorporating biomolecular triggers into functional devices that control electrical, biophysical or biochemical properties. A typical example is a diabetes monitoring device with electrochemical enzyme-based biosensors.

At the core of biohybrid system technology is biosensing which is at the cutting edge of the most recent innovations. It emerged from analytical biochemistry and is of growing interest in many application sectors such as health – both medical and pharmaceutical – security and safety, environment or food quality. There is a strong and rapidly growing demand for small, portable, implantable, fast, reliable and cost-effective sensors and devices. Silicon-based biosensors offer promising perspectives, as they represent an alternative to classical methods with significant advantages in terms of cost and ease of use due to miniaturization and the advantages of batch fabrication. In particular, CMOS-based biosensing is a suitable technology for the design and development of point-of-care (POC) and homecare devices suitable for an emerging mass market.

The ability to design and characterize biohybrid systems is therefore of considerable interest. However, interfacing the biotic and abiotic world remains a challenge since it requires construction and manipulation at the nano- and molecular level. The new Biohybrid Laboratory Facility at the Fraunhofer IMS responds to these requirements by the acquisition of state-of-the-art biochemistry and bioanalytic equipment as well as dedicated instruments for surface characterization.

Figure 1: The Biohybrid Laboratory Facility

Equipment & Instruments

The integration of bioactive elements on microelectronic and micromechanical structures is typically achieved by chemical coupling. The laboratory facility includes equipment for storage, handling and manipulation of biological and biochemical compounds. Biochemical processes can be controlled and monitored using analytical methods such as electrophoresis, spectro-fluorometry and light scattering techniques.

The performance of biohybrid systems is strongly dependent on the quality of the interface between the biological layer and the non-biological substrate. As a consequence the characterization and the quality control of such interfaces is a crucial step in the development of biosensing devices. Two major instruments have been acquired in the Biohybrid Laboratory Facility to address these issues.

First, a high-spec AFM (atomic force microscope) including an optical microscope offers the unique opportunity to combine both AFM measurements with fluorescence microscopy providing information at different scales – the AFM allows the characterization of the sample at the molecular level, whereas the optical microscope allows a more macroscopic charac-

terization. The AFM instrument is optimized for life science systems, in particular performing measurement in aqueous environment. The optical microscope is configured with standard optical techniques, i.e. bright field, phase contrast, fluorescence. The use of such an instrument provides a qualitative evaluation of the "hybridization" in terms of homogeneity, density, and thickness of the functional layer, the topography, and mechanical properties – stiffness, stability, for instance – of the surface.

Second, "biohybridization" protocols can be quantitatively evaluated in terms of bioactivity. Surface Plasmon Resonance is an elegant method to characterize bioactivity, providing information on the equilibrium state constants of the different mechanisms but also on the kinetics of biological processes.

Main goals & Challenges

The specific aim of the Biohybrid Laboratory Facility is to provide technical tools for the design and development of biosensors based on microelectronic and micromechanical systems. This is achieved by interconnecting biological to silicon-based materials in a way that they are able to sense changes and generate a specific response to their environment. In that respect, a certain number of challenges have to be addressed in terms of:

- high specificity for the purpose of the analyses
- stability under normal storage conditions and over a large number of assays
- independence of such physical parameters as stirring, pH and temperature. This allows the analysis of samples with minimal pre-treatment
- accuracy, reproducibility and linearity over the useful analytical range
- for clinical applications, the probe must be tiny and biocompatible, having no toxic or antigenic effects. The biosensor should not be prone to fouling or proteolysis.

The equipment and world-class instruments recently acquired by Fraunhofer IMS allow addressing these challenges. Preliminary investigations for feasibility studies are now available *in situ*. Additionally, characterization of the interface between the biotic and abiotic worlds as well as quality control of the devices is made possible.

The establishment of the Biohybrid Laboratory Facility will have high impact in projects involving the integration of biological and artificial sensing technology. Such projects are already underway and in an advanced stage. An example is a glucose sensing device using tear fluid, based on electrochemical measurements with a single chip nanopotentiostat. In form of a tiny capsule the sensor can be worn for approximately a week under the eye lid constantly monitoring glucose levels and replacing conventional blood based glucose measurement devices. Another example is a sensor for allergen biomarkers which integrates antibodies on top of a polysilicon membrane offering the potential of a highly sensitive and selective detection platform.

Funding

- Lab renovation and installation of 60,000 €
- Investment for Equipment 500,000 €

Summary

The concept of integrating bioactive elements in CMOS-based systems is a key technology for the 21st century and hence of particular relevance to the strategic development of the Fraunhofer IMS. The newly established Biohybrid Laboratory Facility represents a major investment and offers state-of-the-art equipment to industrial and academic partners and collaborators. It offers new and exciting perspectives for biosensing and biotechnology in combination with microelectronic and microelectromechanic system technology in which the IMS is a well established global R&D player. Through new synergies the Biohybrid Laboratory Facility will allow to develop a wide range of new devices, systems and products with enormous commercial potential.

HYBRID SENSOR INTEGRATION BY WAFER-TO-WAFER BONDING

M. Stühlmeyer, A. Goehlich, H. Vogt

Hybridisation by wafer-to-wafer (W2W) bonding is a key technology for the three-dimensional (3D) integration of sensors (or actuators) and ICs. In this process individual wafers are aligned and bonded together by different bonding techniques.
The benefit of this approach consists not only in the fact that different base substrates can be combined, but also different process technologies. The result of theses advantages is the reduction of the process complexity and thereby decreasing the overall process cost. W2W-bonding allows the stacking of substrates nearly without technical limits. After bonding, back-thinning and processing the stack is literally a wafer again and the whole integration process can be repeated several times.

BackSPAD – Hybrid sensor system

In many applications for intelligent sensors or actors the close electrical coupling of the sensing or acting element with the corresponding integrated readout or driving electronics is of great importance in order to minimize the influence of the parasitic impedances of the interconnection. Therefore it is of great advantage to integrate the sensor or actor either monolithically or in a hybrid way with the read out electronics.

The EU funded MiSPIA-project aims at the integration of avalanche diodes on the same substrate comprising the pixel read out electronics. Arrays of Single-Photon Counting Avalanche Diodes (SPAD) smart pixels [1] are generated exploiting in this way the advantages of the CMOS technology combined with near single-photon counting sensitivity. The drawback of this approach is an increased in-pixel circuit complexity, as well as a low fill factor since area is consumed by the sensitive detector matrix that is sited within the read out circuitry. In order to circumvent these drawbacks, a part of the project is dedicated to the development of BackSPAD photo detectors. In this case an array of SPAD photo detectors is fabricated in the 3 µm thick silicon-on-insulator (SOI) film of an SOI wafer with a 0.35 µm feature by the IMS T035 CMOS trench technology. Once processed, the SOI wafer is flipped bonded to a second wafer containing all the required read out electronics, mainly developed for the FrontSPAD smart-pixels. Subsequently, the handle-wafer of the SOI wafer is removed leaving only the high-quality untouched SOI film (together with the buried oxide layer), in which the BackSPADs have been created. In this way the BackSPAD pixels back-side illumination through the left buried

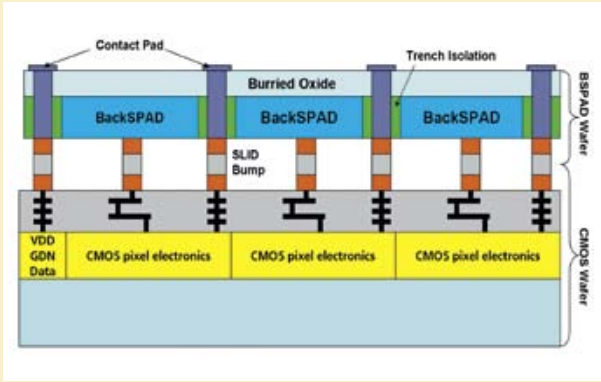

Figure 1: Schematic diagram of the technological cross-section of a BackSPAD smart-pixel array

Oxide (BOX) layer (see Fig. 2) is enabled. This wafer to wafer bonding approach enables the close mechanical and electrical connection of the BackSPAD array and the smart-pixel electronics. The bonding process of the two wafers employs the *solid liquid inter diffusion* (SLID) [2] technique using copper (Cu) and tin (Sn) as the bumping materials.

The SLID bond process

The *solid liquid inter diffusion* (SLID) technique uses copper (Cu) and tin (Sn) as the bumping materials. The main idea of the SLID-process is to utilize two different metallic layers with respectively high (Cu, 1084 °C) and low (Sn, 231 °C) melting points. These layers are brought together into close contact at a temperature above the melting point of Sn. The liquid (Sn) and solid (Cu) phase form one or more inter metallic

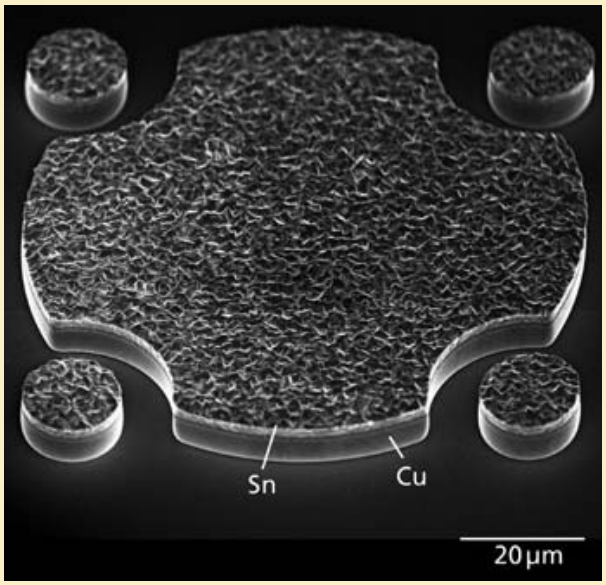

Figure 2: SLID-Bumps after resist removal

compounds (IMC) by inter diffusion. These inter metallic compounds exhibit a remelting temperature between the melting points of the utilized pure metals and in particular exhibit a melting point higher than the process soldering temperature (isothermal solidification). Therefore wafer to wafer bonds can be performed at low solder temperature but can withstand much higher operating temperatures. In order to prevent the diffusion of Cu, a barrier layer made of TiW is sputter deposited first, followed by a sputtered copper-seed-layer for the subsequent Cu- and Sn-plating. Thick resist lithography is utilized to structure bumps and the copper- and tin layers are electroplated afterwards. Figure 2 shows the SLID-bumps after the stripping of the resist by wet chemistry.

In the next process step the seed and barrier-layers are removed in a two step wet etch process. The drawback of using wet etch chemistry is the resulting undercut of the bumps by the Cu-etch solution. As an alternative to the wet etch the ion beam etch technique (IBE) can be used. The advantage of IBE is that no undercut of the Cu/Sn-bumps occurs during the etch process but it exhibits a lower selectivity and the Sn-layer is etched as well. In order to avoid the complete removal of the tin an additional layer of nickel is deposited as a hard masking. The thickness of the nickel is adjusted in such a way, that after removal off the Cu/TiW-layer, the nickel layer is removed as well.

The SLID bonding of the wafers is performed in special designed wafer-bonding system, in which all the necessary steps for the SLID-bonding (i.e.: the wafer alignment with respect of the wafers, annealing sequence and the bonding) can be processed. Special alignment structures are patterned in the bond layers of both wafers. These structures can be easily recognized through by the IR-camera system of the bonder and the alignment can be performed with a high accuracy (< 3 µm). However, this IR-method has few practical limitations. Due to the adsorption of the light in silicon, infrared images are generally possible, if no solid metal layers are overlaid with the alignment key. Another limitation for IR-alignment is smoothness of the entry and exit surface of the wafer stack. A high surface roughness will lead to a blurred image due to light scattering and a backside polish (CMP) is needed to minimize this problem [3].

Following the alignment, the wafers are brought into close contact. Before the tin melts, the surface oxides on top of the metal bumps have to be removed, in order to achieve a clean bond interface. This oxide removal is done with the vapour of formic acid (HCOOH) at a temperature of about 170 °C. At this temperature the formic acid reacts with the metal oxides, reducing them completely to their original metallic stage without any residues. After this step the wafers are heated to the final processing temperature. The tin melts and reacts by inter diffusion with copper and forms the inter-metallic-compounds (IMCs) mentioned above. The melting point of these compounds rises by several hundred degrees and the joints solidifies isothermally at the processing temperature. Figure 3 shows a SEM-image of the bonding interface after solidification.

HYBRID SENSOR INTEGRATION BY WAFER-TO-WAFER BONDING

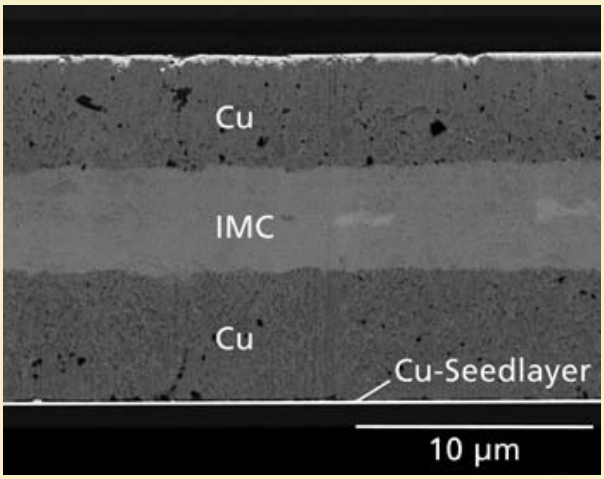

Figure 3: SLID bonding interface after solidification. The inter metallic compounds (IMC) are formed by Cu and Sn.

Wafer thinning and backside contacts

In order to contact the electronic devices, the top wafer is thinned in a two step process. Firstly the SOI-wafer is grinded down to a residual thickness of about 200 µm. The remaining silicon layer can be removed by a highly selective isotropic etch process step (with respect to the oxide) with an etch stop on the buried oxide. The advantage of this two step approach (grinding + etching) is that a huge amount of silicon can be removed in a short time (in addition with a selective etch stop) in comparison to a complete isotropic etch process.

After the thinning process of the BackSPAD wafer the back contact pads for the assembly will be manufactured. First vias will be etched through the buried oxide by a highly anisotropic plasma etch, followed by a metal deposition to fill the via-holes and to form the backside metallization.

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UNCOOLED FAR INFRARED CAMERA BASED ON IMS VGA IRFPA

D. Weiler, M. Petermann

Fraunhofer IMS has developed an uncooled far infrared (FIR) camera for thermal imaging applications like building inspection, pedestrian detection for automotive night vision systems, firefighting, predictive maintenance, quality control and vision enhancement for security and military applications. A FIR-camera detects the emitted FIR-radiation in a scene and displays it as a thermal image by using a PC. The FIR-camera based on a digital VGA-IRFPA (infrared focal plane array) developed by Fraunhofer IMS as the IR-detector combined with an IR lens, a shutter, and the camera electronics. An USB2.0 interface transmits the video data to a PC and receives the configuration data for adjusting the FIR camera.

Introduction

A FIR-camera detects a thermal image of the emitted infrared radiation of a scene similar to a visible camera. Warm bodies like humans or animals emit radiation in the far infrared band (8 µm ... 14 µm) according to Planck's law as a function of their temperature. Due to this emitted radiation an uncooled IRFPA can detect hot spots passively without any active illumination even at worse optical conditions. A FIR-camera estimates the surface temperature of an object due to its infrared radiation and emissivity. Uncooled FIR-cameras use infrared focal plane arrays (IRFPAs) as the image detector operating at ambient temperature. Typical applications for FIR-cameras besides pedestrian detection for automotive driving-assistance systems are thermal imaging, fire fighting, biological imagery, or military applications like target recognition.

Digital VGA-IRFPA

An uncooled IRFPA based on microbolometers is the main component of a FIR-camera and determines the overall electro-optical performance in combination with an IR-lens.

Fraunhofer IMS has fabricated in 2009 the first uncooled infrared focal plane array (IRFPA) throughout Germany. The digital VGA-IRFPAs are completely fabricated at Fraunhofer-IMS on 8" CMOS wafers with an additional surface micromachining process [2]. The IR-sensitive element is realized as a microbolometer based on amorphous silicon as the sensing material. The microbolometer converts the infrared radiation absorbed by a membrane into heat energy and this induces a temperature rise resulting in a change of the electrical resistance. Two SEM images of a microbolometer are shown in Figure 1.

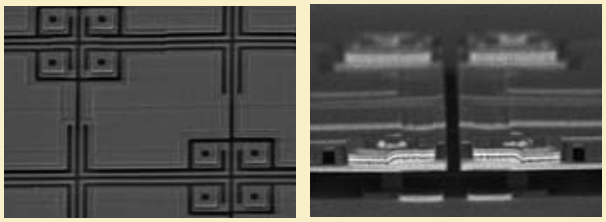

Figure 1: SEM image of a microbolometer (top view and cross section)

The microbolometers are fabricated in a 25µm pixel pitch by post-processing CMOS wafers. The vertical and lateral pixel geometry was kept very simple and straightforward to ensure a solid baseline process with high pixel operability [3].

Microbolometers have to operate in a vacuum-package to reduce thermal losses by gas convection. For reducing packaging costs Fraunhofer-IMS uses a chip-scaled package consisting of an IR-transparent window with an antireflection coating and a soldering frame for maintaining the vacuum [4]. For thermal imaging applications the chip scale package is mounted onto a detector-board as a chip-on-board solution, which is used in a FIR-camera system. The realization of the chip scale package and the detector-board is depicted in Figure 2.

The IR-transparent lid consists of silicon with a double-sided antireflection coating and is placed using a solder frame on top of the CMOS-substrate which includes the readout electronics and the microbolometers. The use of silicon as a transparent lid results in lower production costs compared

UNCOOLED FAR INFRARED CAMERA BASED ON IMS VGA IRFPA

to germanium and causes lower mechanical stress due to equal expansion coefficients between the lid and the substrate.

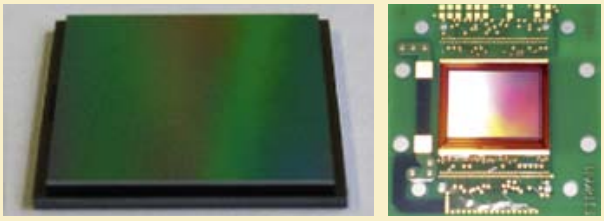

Figure 2: Realization of a chip scale package and a detector board

The chip scale package is currently under development in terms of long-time vacuum stability.

The 640 x 480 microbolometer array is read out by using massively parallel Sigma-Delta-ADCs located under the array which results in a high performance digital readout. Blind microbolometers with a reduced responsivity are located in a ring around the active microbolometer array. The blind microbolometers are read out identically to the active microbolometer. The SD-ADCs convert the scene dependent resistor change directly into 16 bit digital signals. These 16 bit image signals are fed into the digital video interface by a multiplexer. A sequencer controls the readout pattern by selecting each SD-ADC using a line and row control block.

Realization of the FIR-camera

The realized FIR-camera consists of a digital VGA-IRFPA as the IR-detector, an IR lens, a shutter, and the camera electronics. The block diagram of the developed FIR-camera is shown in Figure 3.

The IR-lens focuses the IR-radiation of the scene onto the surface of the digital IRFPA. Typically IR-lenses consist of germanium with f-numbers are used in uncooled FIR-cameras. A shutter is needed for calibration purposes. The shutter is closed periodically approximately every 2 minutes to recalibrate the digital IRFPAs by putting a homogeneous tempered plate in front of the IRFPA and therefore interrupting the IR scene.

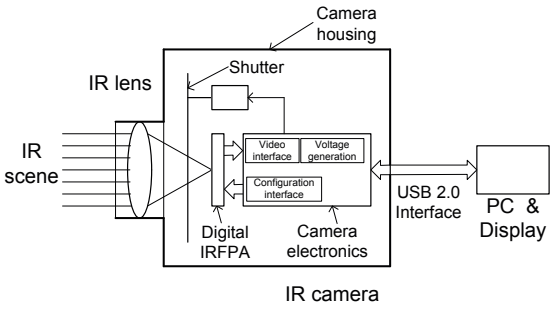

Figure 3: Block diagram of a FIR-camera

The image data of the digital IRFPA are read out by using a camera electronic. The camera electronic consists of three main components: the video interface, the voltage generation, and the camera interface. An USB2.0 interface transmits the video data to a PC and receives the configuration data for adjusting the FIR camera.
The camera electronics consists of two PCBs: an adaptor board and a FPGA board. The camera electronics without shutter and IR-lens is depicted in Figure 4.

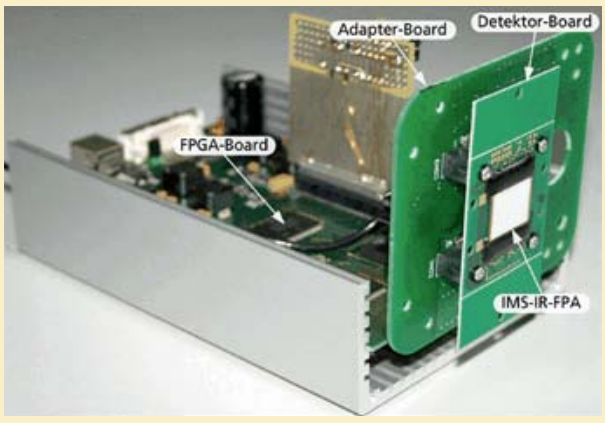

Figure 4: Camera electronics (without shutter and IR-lens)

The first PCB (Adaptor board) generates from one main power supply voltage all required power supply and reference voltages for the digital VGA-IRFPA. A FPGA-board converts the digital video data from the VGA-IRFPA into a USB2.0-videostream. The complete FIR-camera shows Figure 5.

Figure 5: Realized IR-camera

The FIR-camera needs one supply voltage of 12 V and provides the raw digital video data via an USB2.0-interface to a PC, which displays the thermal image after a simple offset correction.

Electro-optical results

An uncompensated IR image of a PC main board taken with the FIR-camera is shown in Figure 6. Apart from a simple offset correction the shown image is uncompensated, i.e. no gain, defect pixel, or noise correction has been done. High temperatures in the scene are displayed as light gray, low temperatures as dark gray.

Hot spots due to high electrical power dissipation can be distinguished from colder regions. In this application failure resulting in a higher temperature can be detected easily by using a FIR-camera.

Figure 6: Uncompensated IR image of a PC main board

Conclusion

Fraunhofer IMS has developed an uncooled FIR-camera for thermal imaging applications. A digital VGA-IRFPA is used as the IR-detector. The video data is transmitted to a PC using a USB2.0-interface. The thermal image is displayed on a PC screen after a simple offset correction. A false color mapping to enhance the thermal image is implemented into the software.

UNCOOLED FAR INFRARED CAMERA BASED ON IMS VGA IRFPA

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AVIONIC DIGITAL SERVICE PLATFORM – AVIGLE

O. Schrey

Unmanned aircraft using wireless communication serving as an „Avionic Digital Service Platform" – AVIGLE – provides 3-dimensional views of individual buildings and even whole city districts while employing the setting-up of a mobile communication platform. Highly precise 3D-Views of geographical interesting areas are nowadays derived from costly aerial photo surveying and an elaborate, often manual post – editing.

1. Project Avigle

1.1 Avionic Digital Service Platform

Unmanned aircraft using wireless communication serving as an „Avionic Digital Service Platform" – AVIGLE – provides 3-dimensional views of individual buildings and even whole city districts while employing the setting-up of a mobile communication platform. Highly precise 3D-Views of geographical interesting areas are nowadays derived from costly aerial photo surveying and an elaborate, often manual post-editing.

The „Avionic Digital Service Platform" AVIGLE realizes this process using small aircraft in combination with state of the art radio communication and image processing technology. A swarm of unmanned aircraft operating at different viewing angles provides the necessary image material and transmits it to a related ground station for further processing. Important application areas of AVIGLE are the so-called "solar potential analysis" of roof areas in citys or the process optimization in disaster control. Avionic Systems provide a quick overwiew over a disaster zone to the rescue teams. In parallel, AVIGLE is capable of providing the rescue teams and the citizens with an ad-hoc mobile communications network compensating the loss of former infrastructure facilities. Within AVIGLE, the new LTE (Long Term Evolution) standard will be utilized based on the innovative 4th generation cellular phone network technology.

Faultless maneuvering in flight requires a dedicated self-sustaining on board flight control. Due to the fact, that an AVIGLE swarm could consist of dozens of flight robots, an efficient and reliable collision avoidance scheme had to be implemented in each flight robot.

Radar systems using reflected radar echo measurement suffer from poor lateral resolution. Time of flight imaging shows significant advantages since the lateral resolution is much higher. Hence, the coarse data of a radar based measurement system would not be applicable for near-field manoevering of an autonomous flight robot system. In contrast, time of flight based vision sensors are able to resolve objects of at least 20 cm x 15 cm size at a distance of 7.5 m.

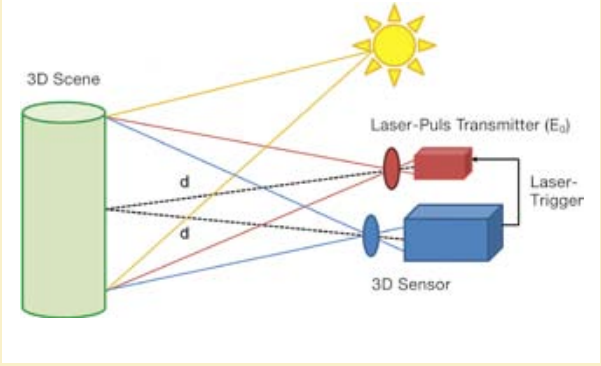

Figure 1: Time of Flight principle

Here, a special 3-D Time of Flight Sensor of Fraunhofer provides the near field (2 m – 8 m) real time surveillance utilizing permanent distance control between the flight robots by emitting pulsed laser radiation and calculating the distance from the back scattered laser light pulse. Figure 1) shows the Time of Flight principle.

2. General Specifications of the 3D Time of Flight Pixel

2.1 Pixel circuit

The developed CMOS-Sensor is capable of measuring 3-dimensional distances by employing laser time of flight principle. Each pixel gray value corresponds with a distance proportion-

ally measurement value obtained by a shuttered or windowed readout scheme. Fig.2) depicts the pixel circuit employing the novel lateral drift field readout scheme. Each measurement cycle charge is accumulated in the FD node and being transferred to the sensor output via a source follower SF. After readout a next measurement cycle is initiated by resetting the floating diffusion node FD by switching ON the reset transistor for a short while, usually in the microsecond regime.

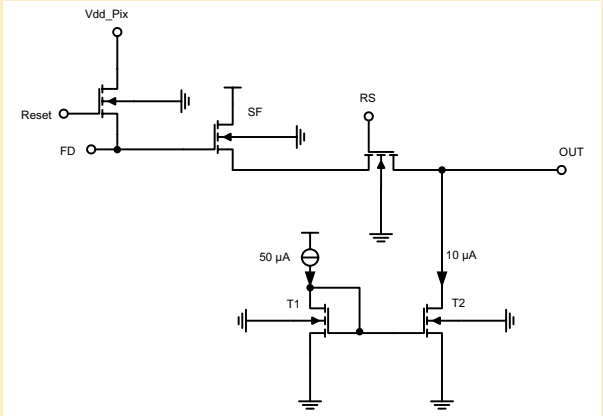

Figure 2: Time of Flight pixel circuit principle

2.2 Time of Flight operation

The distance calculation is done by using three measurements, which are shown in Fig. 3). The reflected laser light pulses ($E_{Laser,snd}$ –> $E_{Laser,rcv}$) are integrated on individual floating diffusion nodes FD1, FD2 and FD3 (not shown) using two measurements including two shutter operations T_{TAP} during Shutter 1 and 2. This requires a replicated pixel circuit structure of Fig. 2) with 1 basic pixel cell for each tap. The first measurement integrates the first portion of the reflected laser light plus the background light for one laser-pulse ($U_{TAP,1}$). The second measurement integrates the remaining portion of the laser light again with background light. ($U_{TAP,2}$). The third measurement detects solely the background light during Shutter 3, since any laser signal should have vanished ($U_{TAP,3}$). A more general use case would add a delay time between Shutter 2 and Shutter 3 or put Shutter 3 before Shutter 1. By employing a significantly high measurement cycle frequency of 20 kHz, fast scene changes are insignificant to the 3D sensor, leaving the three measurement values unchanged.

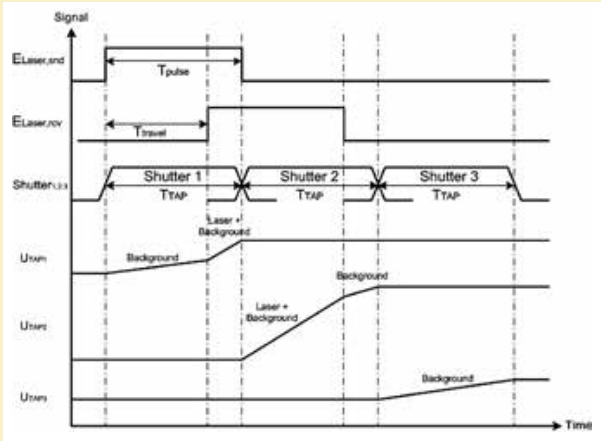

Figure 3: Time of Flight pixel operation

After subtracting the background light from each measurement, the distance is calculated by using the two now background-light-free measurements ($U_{TAP,1} – U_{TAP,3}$) and ($U_{TAP,2} – U_{TAP,3}$). This will be discussed further in detail.
The distance value is computed according to:

$$d = \frac{1}{2} \cdot T_{travel} \cdot v_c \quad (1)$$

With v_c the velocity of light. The background light compensation difference operation is performed by individual subtraction between the corresponding tap values according to:

$$U_{diff} = U_{TAP1} - U_{TAP3} + U_{TAP2} - U_{TAP3} \quad (2)$$

Assuming the reflectivity to be constant and applying the law of photoconversion across a negatively biased space charge region the voltages generated at each tap are given by:

$$U_{TAP} = r \cdot R \cdot E \cdot T_{int} \quad (3)$$

With r representing the object reflectivity, R the pixel responsivity, E the irradiation at the pixel and T_{int} the effective exposure time per exposure signal (laser, background). Employing the laser exposure scheme shown in Fig. 3), the individual tap voltages at the end of one measurement cycle are given by:

$$\begin{aligned} U_{TAP1} &= r \cdot R \cdot \left(E_{BG} \cdot T_{TAP} + E_{Laser} \cdot \left(T_{TAP} - T_{travel}\right)\right) \\ U_{TAP2} &= r \cdot R \cdot \left(E_{BG} \cdot T_{TAP} + E_{Laser} \cdot T_{travel}\right) \\ U_{TAP3} &= r \cdot R \cdot E_{BG} \cdot T_{TAP} \end{aligned} \quad (4)$$

Recalculating (2) using (4) yields for U_{diff}:

$$U_{diff} = r \cdot R \cdot \left(E_{Laser} \cdot \left(T_{TAP} - 2 \cdot T_{travel}\right)\right) \quad (5)$$

Reflectance compensation is achieved by performing:

$$U_{diff1} = U_{TAP1} - U_{TAP3} \quad (6)$$

Division of the two measurement cycles yields the distance proportional factor D:

$$D = \frac{U_{diff1}}{U_{diff}} = \frac{U_{TAP1} - U_{TAP3}}{U_{TAP1} - U_{TAP3} + U_{TAP2} - U_{TAP3}} = 1 - \frac{T_{travel}}{T_{TAP}} \quad (7)$$

Solving (7) for T_{travel} into (1) yields the distance measurement value:

$$d = \frac{1}{2} \cdot v_c \cdot T_{TAP} \cdot \frac{U_{TAP2} - U_{TAP3}}{U_{TAP1} + U_{TAP2} - 2 \cdot U_{TAP3}} \quad (8)$$

Hence, the indirect "Time-of-Flight" is measured by the incoming light within two measurement cycles. This principle is a great advantage of the 3D Sensor chip. It is faster, more accurate and more stable than other technologies.

3. Camera specifications

3.1 Camera and sensor data

In order to fulfill the reliability requirements of the outdoor time of flight operation within AVIGLE, the following key specification criteria have been defined:

Table 1: Key specification data of the ToF sensor and AVIGLE camera

Distance range	0.7 m ... 8 m
Relative distance measurement error	< 5%
Reflectance range	5% – 95% lambertian
Dynamic Range	75dB (distance and reflectance range)
Frame rate	25 fps (up to 128 pulses / frame)
Minimum shutter	30ns
NEP (30ns)	2,3 W/m²
Background light suppression	> 40 dB
Laser wavelength	905 nm
Laser Power	4 x 75 W
Viewing angle	80° h x 18° v
Nominal Ocular Hasard Distance	Laser class 3B / N.O.H.D. = 120 mm
Pixel count	96 x 128
Pixel area	40 x 40 µm²
Fill Factor	33 %
Chip area	6.45 x 6.45 mm²
Process	L035 CMOS OPTO

The following figure shows the chip micrograph.

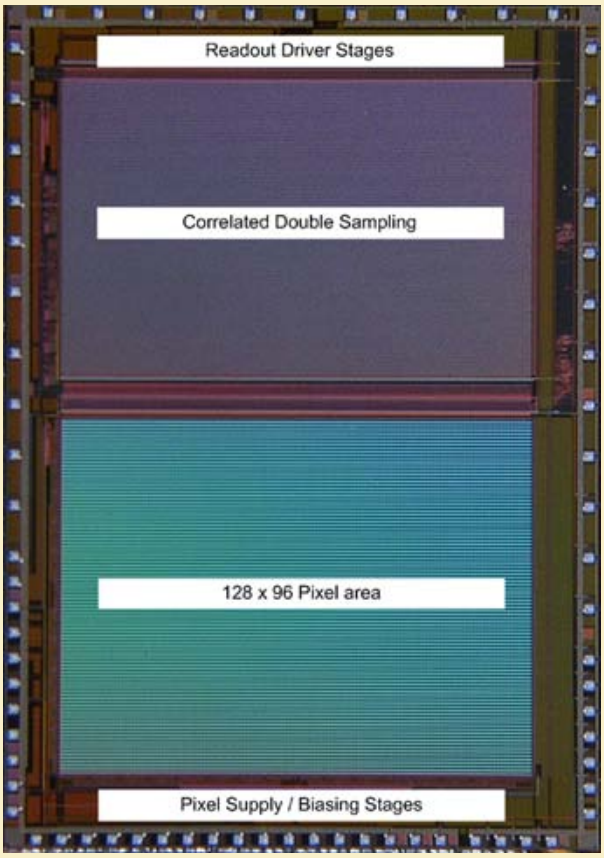

Figure 4: Chip micrograph of the AVIGLE time of flight sensor

The hardware of the camera consists of 4 fundamental components which all have been developed within the AVIGLE project:

1. Customized 96 x 128 pixel 3D-CMOS chip with sensor electronics
2. Imaging optics
3. 4 x 75 W Laser modules for active infrared illumination
4. Laser optics for the beam forming of the laser illumination
5. Customized Ethernet IF
6. Custom EIA485 IF to flight control

The mechanical assembly of these components into a common housing has been designed to be in line with the requirements of the mounting restrictions of the front nose of the flight robot. Fig. 5 shows the Time of Flight camera mounted in the front part of the flight robot directly looking at the observed image scene.

Figure 5: Time of Flight Camera mounted in the front of the AVIGLE module

4. Distance measurement characterization

In order to characterize the distance measuring performance of the CMOS camera, the measured accuracy and repeatability of the distance data has been evaluated for various target objects, which have been positioned in a distance range from 1 m to 7 m.

Fig.6 illustrates the mean distance values d_m derived from a statistically relevant set of measurement data for a plywood target with a Lambertian reflectivity of ~ 50 %. A central pixel of the imager array is considered.

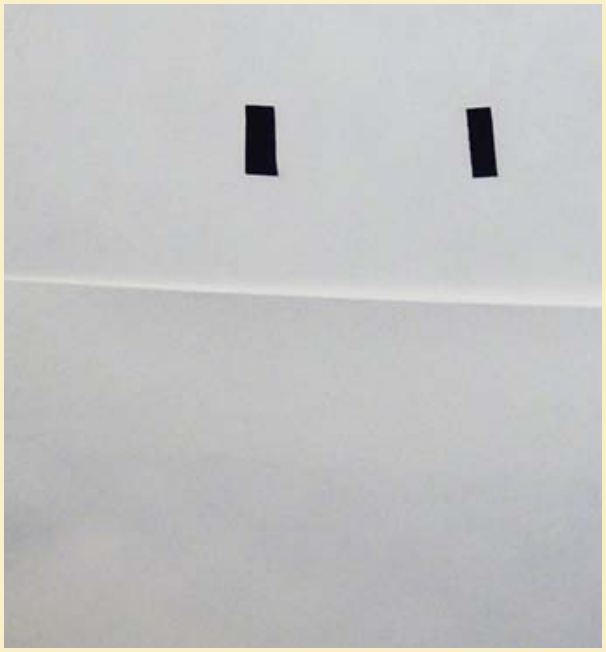

Figure 6: Measured target with 70 cm x 90 cm white background and 2.5 cm x 5 cm black stripes

The following figure shows the output values of TAP1 and TAP2 on the left hand side, and the quotient factor D on the right hand side.

The measurement series of the distance proportionally values is (28, 41, 54, 60, 66, 70, 75) for the pre-set distance values of (1 m, 2 m, 3 m, 4 m, 5 m, 6 m, 7 m). The non-linear characteristic reveals a required further refinement of the reflectance compensation operation along with a further sensor linearization. These tasks are currently under development.

5. Summary and Outlook

Taking advantage of the accumulation capability of the floating diffusion node of the time of flight image sensor, a fixed number of back-scattered laser pulses has been accumulated for each pixel. Future developments include the introduction of multiple pulse accumulation at various, but fixed accumulation numbers. Using a set of 1, 4, 8, 32 and 64 discrete accumulation steps, the signal-to-noise ratio will be further optimized for each pixel thus leading to a distance accuracy which is almost independent from the target distance, despite of the fact that the back-scattered light received by the sensor pixel decreases with the square of the distance.

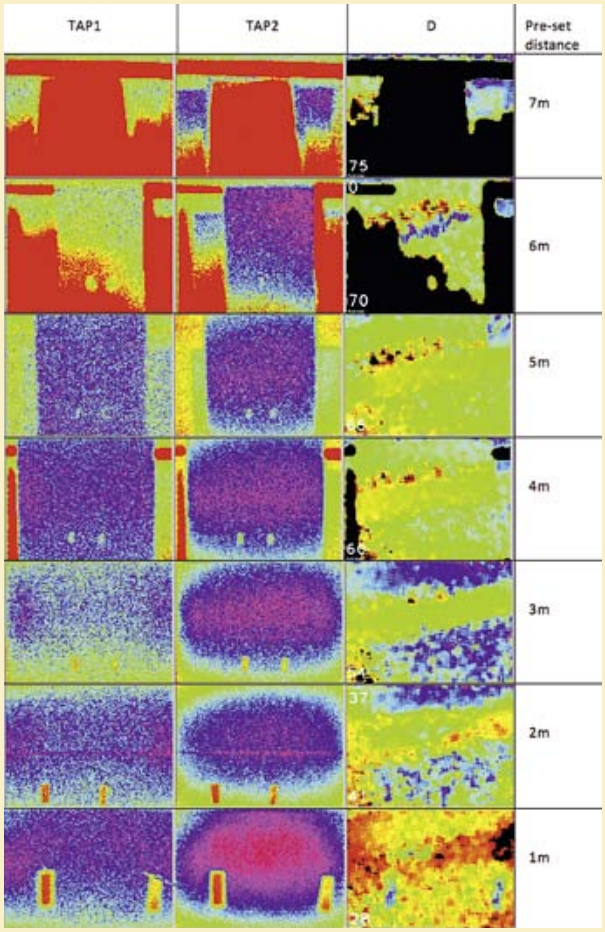

Figure 7: Distance range measurement from 1 m … 7 m

INTEGRATED CMOS SINGLE PHOTON AVALANCHE DIODES

D. Durini, S. Weyers

For a vast number of applications ranging from spectroscopy, fluorescence life-time imaging (FLIM), positron emission tomography (PET), to time-of-flight (TOF) principle based ranging and three-dimensional (3D) imaging, the capability to count single photons in extreme short periods of time (in range of picoseconds) is the main requirement. For many years, this extreme time-resolution with the proper spectral sensitivity was only possible by using Photomultiplier Tubes (PMT) or Micro-Channel Plate (MCP) technologies. The main disadvantages of these two mature technologies are nevertheless their high electromechanical complexity involving the need for biasing in ranges of thousands of Volts and their practically non-existing spatial resolution. Even special modified semiconductor technologies involving charge-coupled devices (CCDs) and CMOS based active pixel sensors (APS) were up to now not capable of achieving the requirements for spatial resolution and photon counting simultaneously, and the required time-resolution was almost completely out of reach.

At the beginning of the 21st century the first concepts were defined to emulate the performance of PMT and MCP technologies, but profiting of the cost-performance ratio, the yield, and the maturity of the silicon based semiconductor fabrication: the concept of Single-Photon Avalanche Diodes (SPADs) capable of both, high time – resolution and also high spatial resolution, was defined and has been continuously optimized. On the other hand, a parallel PMT silicon based equivalent called Silicon Photomultiplier (SiPM) was conceived and fabricated, delivering picosecond time-resolution and simultaneously a spatial resolution higher than that of the PMTs, but still much poorer than in the case of the SPADs.

At the Fraunhofer IMS we incorporated process modules to our standard CMOS technologies that enable fabricating integrated SPAD structures, as it will be described below. This development was undertaken in frame of the "MiSPiA" project under the ICT theme of the EC 7th Framework Program (FP7, 2007 – 2013), under the grant No. 257646. Our partners, Politecnico di Milano and Micro Photon Devices S.r.l. are the responsible partners for the complete circuit design of the SPAD sensors fabricated in the specially developed IMS SPAD technology.

Integrated SPAD device

The SPAD device consists of the *pn* junction of a highly doped *p* layer in a deep *n*-well which is reverse biased well beyond its breakdown voltage. It is thus operated in the Geiger-mode where an electron hole pair generated by a single photon ignites a charge carrier avalanche. In order to confine the electrical breakdown to the active area of the SPAD a lowly doped *p* guard-ring surrounds the junction and an *n* implantation increases the electrical field in the active device area (Fig. 1). The *n* implantation is also used to adjust the breakdown voltage of the device.

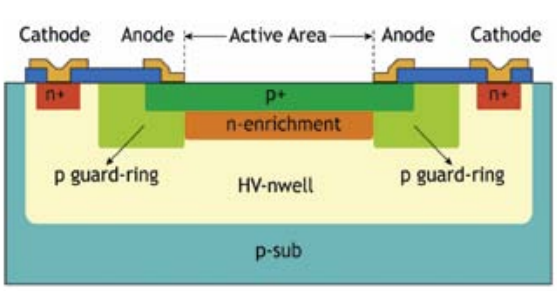

Figure 1: Schematic cross section of an integrated CMOS SPAD device [3]

The current which results from triggering of an avalanche has to be quenched and subsequently the operational bias has to

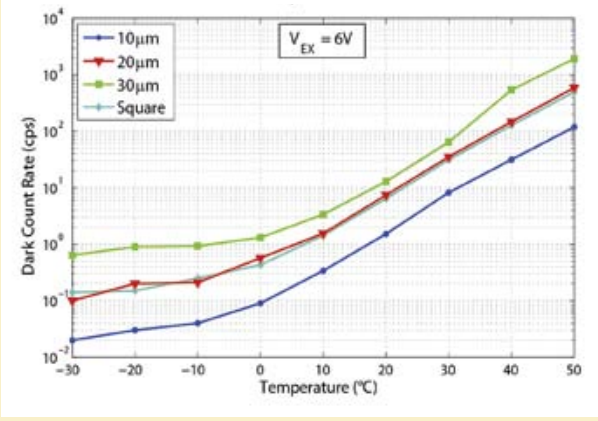

Figure 2: Dark count rate as a function of the temperature for different device diameters [3]

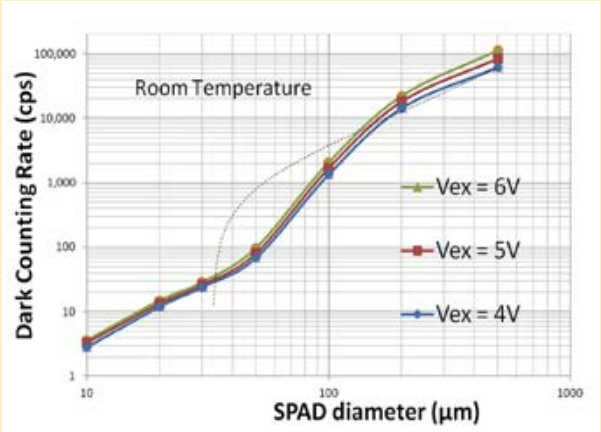

Figure 3: Dark count rate as a function of the SPAD diameter for different excess biases at room temperature

be applied again in order to be able to detect further photons. The quenching is done by an active quenching circuit which allows making the device sensitive to new photons within a few tens of ns after the detection of a photon. The macroscopic current generated by the avalanche and the point in time it occurs can easily be detected by a readout circuit. The intensity of the impinging light is determined by counting the number of detected photons. Since the SPAD is biased beyond the breakdown voltage the ignition of an avalanche is not restricted to a free charge carrier generated by the absorption of a photon. Thermally generated charge carriers that reach the high electric field region of the SPAD will also trigger an event. The rate of intrinsically generated events is measured as the dark count rate (DCR) and determines the signal to noise ratio of the device.

Results

The integrated SPADs were fabricated in a 0.35 µm CMOS technology. Test structures consisting of single SPADs with as well as without quenching circuits were fabricated to characterize these devices.

The breakdown voltage of the SPAD device was measured to be 25 V. The dark count rate of the SPAD as function of temperature and excess bias, which is the difference between the applied bias voltage and the breakdown voltage, is shown in Fig. 2. With a value of 20 cps for a 30 µm diameter SPAD at room temperature the DCR is very low compared to state-of-the-art SPADs fabricated in a different 0.35 µm technology [1]. For low temperatures the DCR decreases to 1 cps for temperatures of 0 °C and below. Due to the low DCR the SPAD diameter can be increased to gain a higher fill factor and higher sensitivity. Even for 80 µm diameter SPADs the DCR is below 1000 cps (Fig. 3).

The spectral sensitivity is shown in Fig. 4. At 400 nm wavelength the device has its highest photon detection efficiency (PDE) of 40 % to 50 % depending on the excess voltage. For longer wavelength the PDE decreases, but still achieves 10 % at 740 nm. The PDE decrease is mainly related to the decreasing absorption in Silicon for longer wavelengths and the limited depth of depletion region defined by the used n-well. All photons which are absorbed in the Silicon below the depletion region will not trigger an avalanche and therefore are not detected. Shorter wavelengths could not be applied due to the used spectrometer, but from results ob-

INTEGRATED CMOS SINGLE PHOTON AVALANCHE DIODES

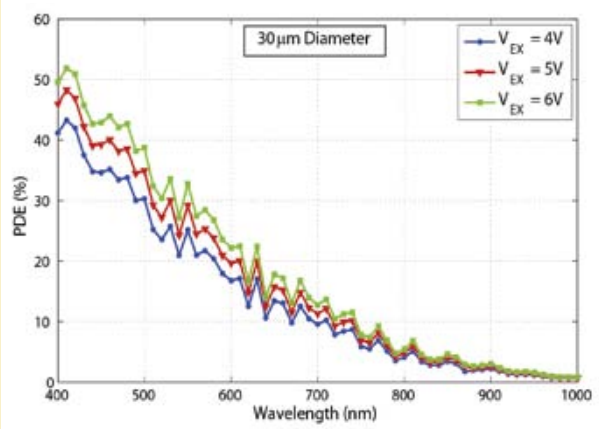

Figure 4: Spectral photon detection efficiency (PDE) for different SPAD diameters [2]

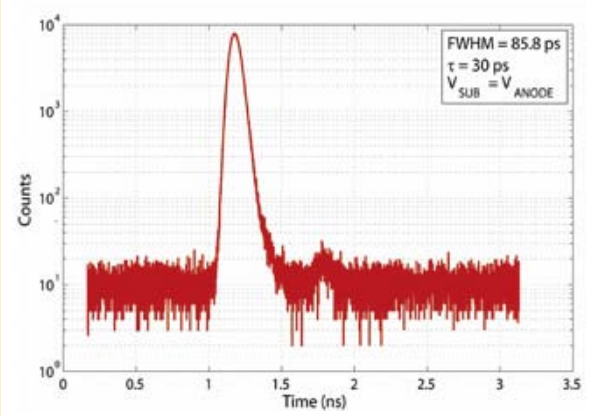

Figure 5: Timing waveform of the signal generated by a photon and quenched by the applied quenching circuit [3]

tained from CMOS photodiodes fabricated in the same technology a significant decrease of the detection efficiency could only be observed for wavelength below 300 nm. The time resolution of a SPAD including quenching circuit is below 100 ps (Fig. 5).

In addition to these test structures full imagers with readout circuit and interface were fabricated.

In standard CMOS imagers the information of each pixel consists the charge generated by impinging photons and the pixel consist of the photodiode and a few transistors for reset and selection. For the pixel in a SPAD imager the stored information is the number and the time of detected photons. Therefore, each pixel has to contain a counter, memory, buffer and a quenching circuit. For TOF applications the pixel can contain even more than one counter. In combination with the dimension of the SPAD structure itself this adds up some area required for each pixel. While in the applied 0.35 µm technology the pitch for CMOS pixels is in the order of 10 µm the pitch for SPAD pixels is in the order of 100 µm.

Imagers with 64 × 32 SPAD dual function smart pixels were fabricated which can be used for "*photon counting*" application like high sensitive 2D imaging as well as "*photon timing*" application like 3D TOF [2]. It is even possible to combine these two operational modes to get distance as well intensity information from the observed scene. In the photon timing mode the imager achieves a spatial precision of less than 10 cm, limited by the time resolution of the used Time-to-Digital Converter of 312 ps.

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HIGH TEMPERATURE ANALOG-TO-DIGITAL CONVERSION UP TO 250°C IN A SOI CMOS PROCESS

A. Schmidt

Silicon-on-Insulator (SOI) CMOS is the most commonly used technology for integrated circuits suitable for high temperature and harsh environmental conditions. Data acquisition circuitry operating at these conditions has to consider the impact of wide temperature range operation. Therefore, the accurate operation of elementary building blocks is essential for high system performance. To overcome the accuracy limitations set by channel leakage and performance degradation of NMOS and PMOS transistors, advanced circuit design methods are necessary. By introducing advanced leakage compensation, the overall performance of analog circuits at elevated temperatures is significantly improved. The cyclic analog-to-digital converter presented here has a resolution of 12 bit and is fabricated in the Fraunhofer IMS 1.0 µm SOI CMOS process. It utilizes the redundant signed digit (RSD) principle in a switched capacitor circuit and is thus insensitive to amplifier or comparator offset. In order to reduce the conversion error, leakage current compensated switches have been used. The ADC is intended as an IP module to be used in customer specific mixed signal integrated circuits.

Introduction

Analog and mixed-signal circuit design for a wide operating temperature range, reaching from – 40 °C up to 250 °C, is strongly affected by temperature dependencies of basic analog circuits and increasing leakage currents. Within a wide temperature range circuits have to meet requirements like high accuracy and fast operating speeds while specific circuit techniques like the switched capacitor (SC) technique are preferred for integrated circuit design. Better matching capabilities, capacitor ratio independent circuit topologies, built-in offset cancellation and decreased power consumption are beneficial also at high temperatures.

In the design approach increased leakage currents and decreased transistor performance, i. e. intrinsic gain and intrinsic bandwidth have to be considered for high temperatures. Transistor channel leakage currents in analog switches within these SC circuits lead to decreased accuracy as charges leak from or onto storage capacitors.

Therefore analog circuit design up to 250 °C has to consider leakage currents as a major source of conversion error in analog-to-digital converters (ADC) utilizing SC circuit technique. Since technology improvements are only capable of reducing leakage currents by a limited amount, novel design techniques are required to eliminate the resulting effects through improved circuit design techniques. This implies the reduction of leakage currents within the capabilities of circuit design in the first place and secondly the compensation of remaining leakages by compensation structures brought into the circuit. Improving intrinsic gain and bandwidth at high temperatures is also to be realized by using novel design techniques.

Solving these issues will allow precision analog circuit design for a wide temperate range. The circuit presented here is a single ended cyclic RSD analog-to-digital converter fabricated in the Fraunhofer IMS 1.0 µm SOI CMOS process. Compensation of leakage currents at high impedance nodes inside the ADC to improve its accuracy at high temperatures is discussed and verified by measurement results.

Principle of analog to digital conversion

The 12 bit cyclic RSD analog-to-digital converter presented here features a sample rate of 1.25 kS/s with an input signal range from 0 V to 5 V. The ADC has to operate properly in a temperature range of – 40 °C up to 250 °C. It is realized in SC technique. Due to RSD code usage, the ADC is able to correct earlier false decisions by the ADC's comparators and to convert an analog input signal within 11 cycles into a 12 bit digital result [1-3].
Figure 1 shows the circuit implementation of the ADC's analog core.

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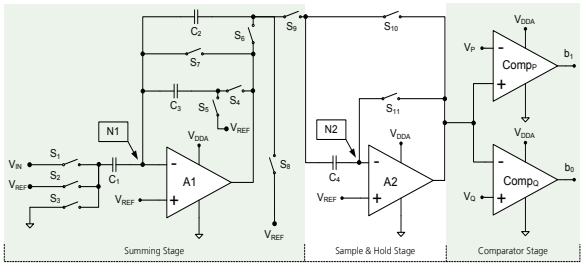
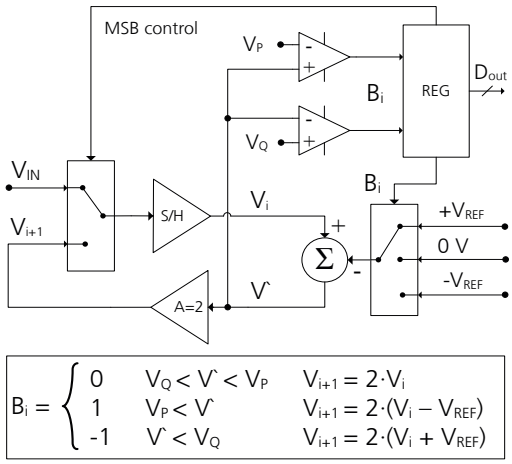


Figure 1: Topology of the proposed 12 bit cyclic RSD analog-to-digital converter [5].

A summing stage formed by operational amplifier (Op-amp) A1 and switches $S_1 - S_8$ executes arithmetic operations, i. e. multiplication by a factor of 2 and the subtraction / addition of the reference voltage VREF from / to the residual voltage during conversion. The second stage consisting of amplifier A2 and switches $S_{10} - S_{11}$ forms a sample and hold stage for the output voltage of the summing stage. The comparator stage compares the sampled voltage against two reference voltage levels V_P and V_Q. The analog-to-digital conversion principle is given in Figure 2.



$$B_i = \begin{cases} 0 & V_Q < V` < V_P \quad V_{i+1} = 2 \cdot V_i \\ 1 & V_P < V` \quad V_{i+1} = 2 \cdot (V_i - V_{REF}) \\ -1 & V` < V_Q \quad V_{i+1} = 2 \cdot (V_i + V_{REF}) \end{cases}$$

Figure 2: Principle of the analog-to-digital conversion [5].

As one can see in Figure 2, the input voltage V_{IN} is first sampled and then compared to VREF using two thresholds V_P and V_Q yielding the MSB (most significant bit) of the conversion result. The digital result D_{OUT} is held in a register within the digital part of the ADC. The residual voltage V_i+1 of the next conversion cycle is then derived from V_i by subtracting or adding V_{REF} dependent on the voltage level of V_i. The result is then multiplied by a factor of two. This residual voltage V_i+1 is sampled and compared to V_P and V_Q. All successive bits are then calculated analogously to the prior described cycle. The operation principle illustrated in Figure 2 is implemented in the analog core of the ADC by controlling the switches $S_1 - S_{11}$.

For the sample and hold functionality as well as for the basic arithmetic operations, two precise operational amplifiers are necessary. To ensure a precise operation of the analog-to-digital converter, a minimum DC gain of 90 dB is desired even at high temperatures. This is realized using a gain-boosted operational amplifier with a rail-to-rail output stage [4]. Since the offset of both op-amps is eliminated during the conversion cycle [1], there is no need to cancel the offset of the amplifiers itself.

Leakage current compensated analog switch

Increased leakage currents at high temperatures lead to decreased accuracy as charges leak from the storage capacitors within the switched capacitor circuit. Especially at high impedance nodes within the ADC circuit, the leakage behaviour of switches connected to these nodes mainly determines the conversion error. In the ADC presented in Figure 1 there are two high impedance nodes N1 and N2 when S_7 and S_{11} are turned off. Since nodes N1 and N2 are the virtual ground of the amplifiers A1 and A2 respectively, they remain at V_{REF} in feedback configuration. As charges intend to leak from or onto the plates of C_2, C_3 and C_4 dependent on the output voltage of the amplifiers A1 and A2, switches S_7 and S_{11} need to be optimized towards low leakage currents.

Figure 3 shows a regular bidirectional transmission gate (left) using HGATE transistors and a leakage current compensation

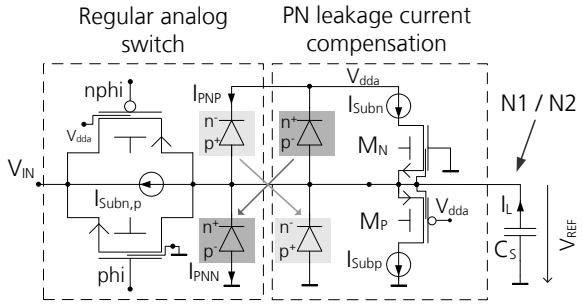


Figure 3: Leakage current compensation for the analog switch [5].

structure (right). The HGATE itself is a bidirectional device with a separate film (body) contact. It is worth noting, that leakage currents at these nodes has been determined as the dominating source of error. At the nodes N1 / N2 charge injection has been therefore neglected but is considered in all switches other than S_7 and S_{11}. Two leakage current mechanisms dominate the overall leakage behaviour at high temperatures: the subthreshold leakage current I_{Sub} and the pn-junction leakage current I_{PN}. The leakage current I_L discharging the capacitive load C_S is a combination of both leakage mechanisms and is thereby dependant on the voltage difference $V_{REF} - V_{IN}$ and the operating temperature.

Thereby V_{IN} can vary between 0 V and V_{dda} depending on the input voltage of the analog-to-digital converter. Comparing I_{Sub} and I_{PN} in magnitude, the subthreshold leakage current I_{Sub} dominates at high temperatures and 0 V gate-source-voltage. Once the gate-source-voltage for the NHGATE or PHGATE turns negative or positive respectively, the subthreshold leakage current is significantly reduced in both devices.

To further reduce the subthreshold leakage current $I_{Subn,p}$ and also to prevent short channel leakage effects like DIBL (drain induced barrier lowering) minimum channel length has been avoided. The pn-junction leakage current remains active after reducing the subthreshold leakage current. Both parasitic junction diodes are shown in Figure 3.

Since the parasitic diodes are different in doping concentration, the reverse leakage currents will not match. As a consequence I_L will be different from zero leading to a discharge or charge of the capacitor C_S. Complementary parasitic diodes add to the existing ones by bringing in a compensation structure consisting of the transistors M_N and M_P. The body contacts of M_N and M_P are connected to N1 / N2. As one can see in Figure 3a the voltage across the parasitic diodes of the switch and its compensation counterparts are equal, i. e. V_{REF}. Thereby a mismatch in pn-junction leakage due to different junction voltages is avoided. In case all transistors are matched properly in size and layout, leakage currents in the complementary parasitic diode structures would cancel. The remaining pn-junction leakage is reduced by several orders of magnitude. The compensation transistors M_N and M_P themselves bring subthreshold leakage currents into the nodes N1 / N2.
Due to the back-gate-effect, which is responsible for a shift in threshold voltage of the PMOS device, the corresponding subthreshold leakage current can be significantly higher than in the NMOS.

Given that the gate-source-voltage of M_N and M_P is $\pm V_{REF}$ the subthreshold leakage currents of both compensation transistors are effectively reduced. Using the compensation method presented here the overall leakage current at the nodes N1 / N2 has been reduced yielding a lower conversion error at elevated temperatures.

Experimental Results

In this section experimental results of the ADC are presented. In Figure 4 the conversion error $V_{IN} - V_{OUT}$ compared to the ideal transfer function at 25 °C and 250 °C are shown. The offset- and gain error derived from Figure 4 for an operating temperature of 25 °C is found to be – 8 mV with a gain error of 1.0056. At a temperature of 250 °C the offset- and gain error is 7.9 mV and 1.0021 respectively. Figure 5 presents the

HIGH TEMPERATURE ANALOG-TO-DIGITAL CONVERSION UP TO 250°C IN A SOI CMOS PROCESS

differential non-linearity (DNL) and the integral non-linearity error (INL) at 25 °C and 250 °C. At 25 °C the maximum INL is 1.2 LSB.

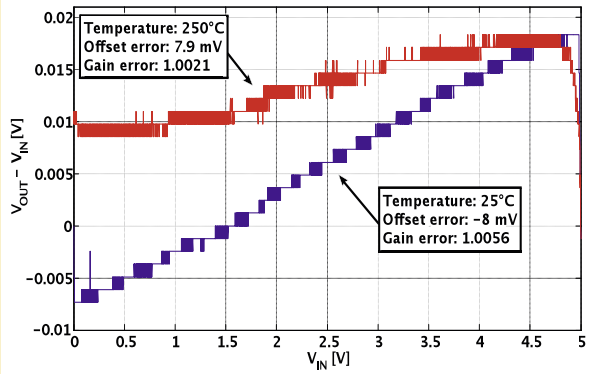


Figure 4: Conversion error in comparison to ideal transfer function [5].

Table 1: ADC specifications summary [5].

Temperature range	−40 °C to 250 °C
Voltage supply	5 V
Sample rate	1.25 kS/S
Power consumption (analog part)	3.4 mW @ 25 °C
Input voltage range	0 V / 5 V
Resolution	12 bit
Offset error	−6.5 LSB @ 25 °C 6.5 LSB @ 250 °C
Gain error	1.0056 @ 25 °C 1.0021 @ 250 °C
INL @ 12 bit	1.2 @ 25 °C 2.0 @ 250 °C
DNL @ 12 bit	max. 0.5 @ 25 °C max. 1.5 @ 250 °C
Area	1.85 mm²

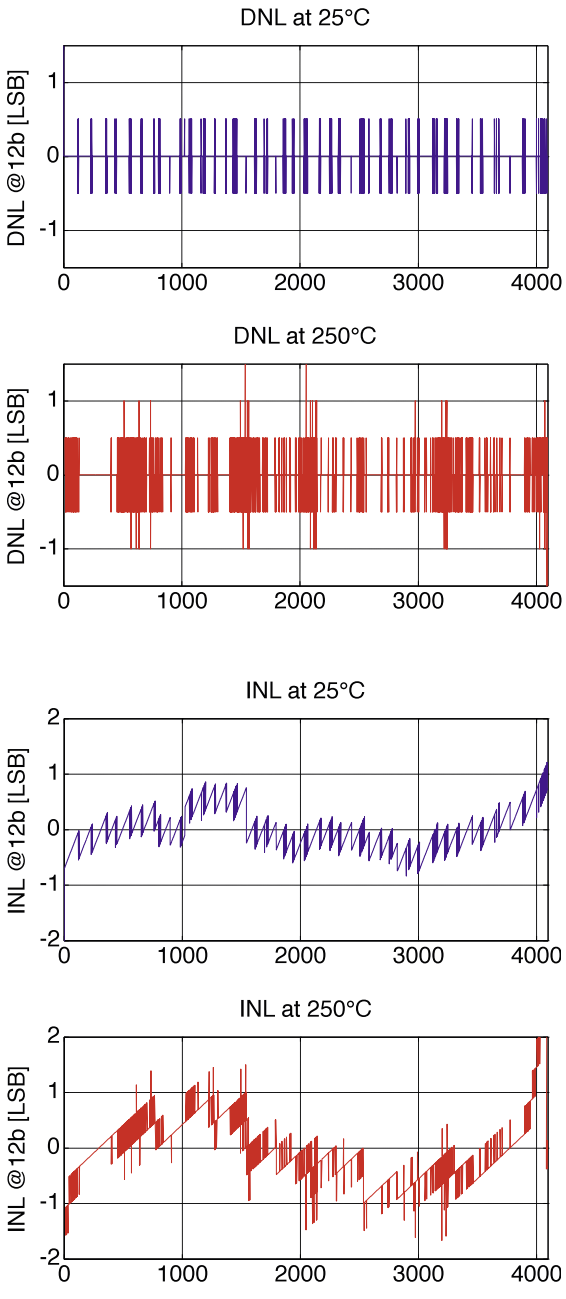


Figure 5: INL and DNL @ 12 bit for 25 °C and 250 °C [5].

At high temperatures the maximum INL at high input voltages is found to be 2 LSB. Due to increased noise level at high temperatures mean values were extracted from the performed measurements yielding a decreased sample rate. Table 1 summarizes all experimental results. With a supply voltage of 5 V the analog core of the ADC has a power consumption 3.4 mW measured at room temperature. A chip photo of the ADC's analog core is shown in Figure 6.

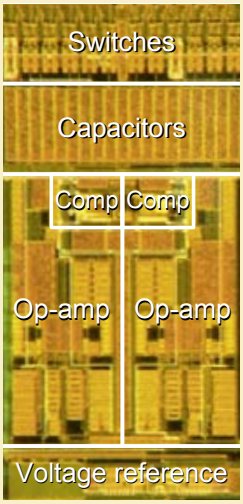


Figure 6: Chip photo of the ADC's analog core [5].

Conclusion

A single ended 12 bit cyclic RSD analog-to-digital converter targeting high temperature range applications up to 250 °C has been presented. Due to the fact that high leakage currents in analog switches degrade the ADC's accuracy at high temperatures, a current compensation scheme to reduce the overall leakage currents has been presented. The proposed compensation scheme has been implemented at high impedance nodes inside the ADC. Measurement results show the expected performance over the whole temperature range up to 250 °C.

Further improvements of the overall performance, e. g. decreased noise level at elevated temperatures and decreased charge injection within the leakage compensation scheme are currently investigated. For that purpose improvement in device parameters regarding effective noise and using a differential approach is intended. The ADC is available as an IP module to be used in customer specific mixed-signal integrated circuits.

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DC/DC CONVERTER

A. Stanitzki

Point-of-load converter with digital control loop

Today, supply voltage for battery powered devices is commonly generated using efficient switch-mode converters, so called DC/DC converters. In other applications, there is a trend from using a centralized power supply block towards distributed supply concepts with local regulators (point-of-load). These distributed architectures are programmed and monitored via digital control busses and hence, nearly all commercially available DC/DC converters incorporate one or more digital interfaces like I²C or its specialized derivate SMBus.

While digital system components are fully affected from the shrink in feature sizes when process technology advances, typical analog parts of the control loop like sawtooth generators, filters and especially the actual power switches don't scale well and hence dominate the overall die area. To encounter this, specialized process technologies are developed, combining dense CMOS logic with high voltage tolerant switching devices like LDMOS, which also provide optimized device parameters concerning RDSON and input capacitance.

In cooperation with a french Semiconductor (a specialty foundry based in Paris/France) Fraunhofer IMS has developed a DC/DC buck-converter using a fully digital control loop which can be monolithically integrated with Altis proprietary LDMOS power switches to target a 2 Watts output power range. By using a digital-only approach the high logic density of the process can be exploited while the power devices allow for an operating input voltage range of up to 12V and above.

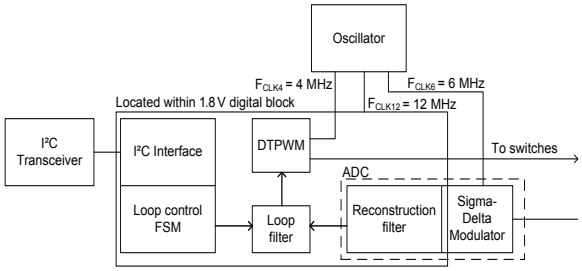

Figure 1: Block diagram of the DC/DC converters control loop

A simplified block diagram of the control loop is given in Figure 1. The output voltage is generated by switching the power devices using a pulse-width or pulse-density modulation scheme. The modulator consists of an m-bit sigma-delta modulator which transforms a 10 bit wide digital target value into an n-bit data-stream with increased sample rate. The number of quantisation steps is programmable, hence a seamless transition from pulse-width to pulse-density modulation can be realized, as it is required for efficient conversion at different load levels.

The feedback path is provided by an ADC which is also based on a sigma-delta principle. The reconstruction filter and loop filter are included in a logic block. The control parameters – e.g. target output voltage and filter gains, resolution of sigma-delta modulator, switching-frequency – can be user-defined via an I²C-interface.

Figure 2 shows the floorplan of the converter and pin locations for a QFN48 package option. High voltage components and logic are separated by special guard structures (guard rings and trenches) to minimize crosstalk and substrate noise.

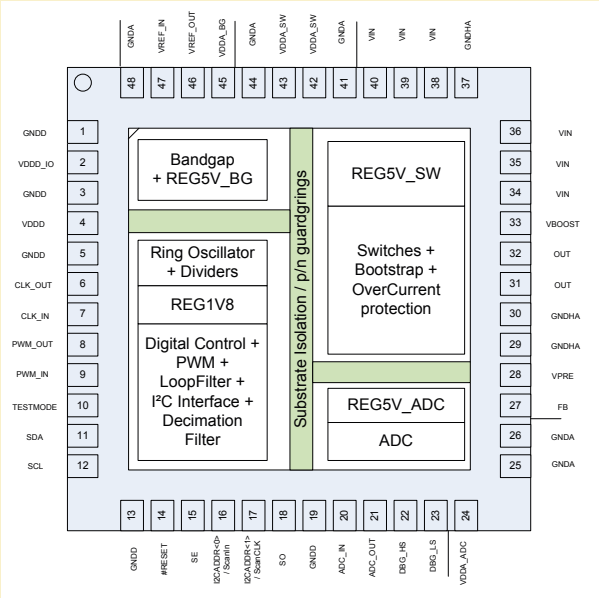

Figure 2: Floorplan and possible pin-out for QFN48 package option

The target specification for the converter is 90 % conversion efficiency at 1A output current in a programmable output voltage range of 2.5 V – 10 V (12 V input). Short circuit and overvoltage protection are included and the switching frequency can be selected as 125 kHz, 250 kHz or 500 kHz.

FLEXIBLE DEVELOPMENT AND TESTING ENVIRONMENT FOR IMPLEMENTATION OF NEW ALGORITHMS IN RFID SYSTEMS

S. Grey, G. vom Bögel, A. Grabmaier

This paper presents a rapid-prototyping platform for test and implementation of new algorithms in RFID Systems. The platform offers the possibility to evaluate and test new approaches, in communications aspects in RFID systems, that can not be tested in state-of-the-art systems, due to hardware or standards limitations. This includes new radio architectures, source-/line-coding schemes, multiple access control algorithms and many other system elements that can not be accessed or changed in a RFID system. Two platforms are presented: one for algorithm development and a second one for product development. Full article and references in [1].

I. INTRODUCTION

A. Radio Frequency Identification

In the last years RFID has evolved into an active multidisciplinary area of research and development, composed by a broad spectrum of fields. The tasks of RFID tags have become more complex, this includes:

- Tags are placed in reflective environments.
- Tags are provided with sensor capabilities used to monitor specific processes.
- Higher data rates are needed in systems where the tag sends more than just its ID, i.e. sensor tags.
- The reliability of RFID systems has to be increased. The user needs to be sure that all tags are read at all times.

All these challenges have open the doors for research and development in the areas of RFID. Many algorithms and technologies of other communication areas are being applied to RFID systems. Nevertheless in order to evaluate new ideas in RFID a prototyping system is needed, one which provides flexibility and the possibility to work outside of the standards and state-of-the-art systems.

B. SDR in RFID

The idea of using SDR in RFID for prototyping has been already explored in different publications [1]. In this publications the authors have used the flexibility of SDR to test new coding schemes, radio architectures, channel equalization, new modulation schemes, MIMO approaches and other research activity.

II. RAPID PROTOTYPING PLATFORM

This paper presents a rapid-prototyping platform for test and implementation of new algorithms in RFID Systems. This section gives a basic description of the main elements and capabilities of the platform. Two platforms have been developed. One for research and development and another one for fast product-prototyping.

A. Structure

The Figure 1 presents an overview of the main components of the test platform. The main element is the FPGA which is where the signal processing takes place. There is a fast digital interface where transmitter and receiver can be connected to. The PC can communicated with the FPGA in order to configure it of control a certain action. The transmitter and receiver configuration depends on the RFID technology in use.

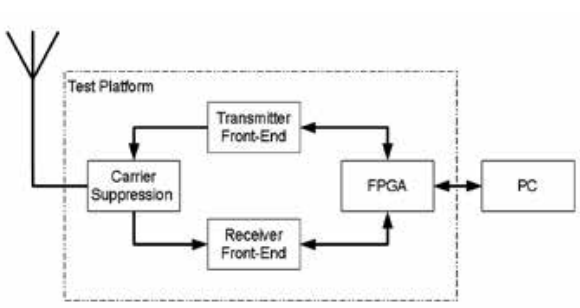

Figure 1: Overview of the Test Platform

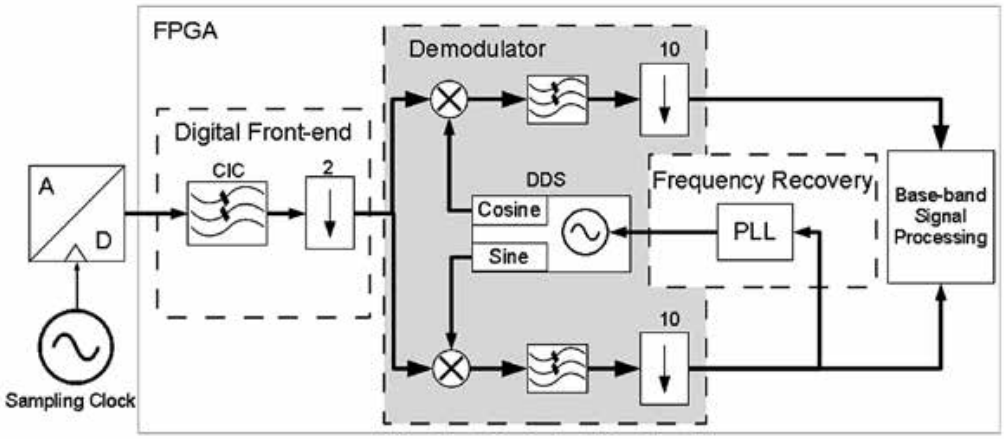

Figure 2: Digital Front-End Flow Diagram

B. Hardware Elements

1) Signal Processor: In the center of the test platform is the signal processor. The signal processing is done in the digital domain, this adds flexibility to the system. The processing algorithms are defined in software.
FGPA: The signal processor chosen for the test platform is an FPGA. The FPGAs used in both boards have a high number of logic elements.

2) Analog Digital Converter: To add flexibility to the system, most of the signal processing would take place in the digital domain. Therefore an analog to digital converter (ADC) works as interface between the analog signal processing and the digital signal processing. There are two ADC modules that can be adapted to the test platform, their use depends on the desired configuration of the system.

12 bits @ 500 MSPS: One of the ADC modules can sample signals up to 500 MSPS (Mega Samples Per Second) and has a resolution of 12 bits. The resolution of this ADC module could be of a disadvantage when sampling signal with a high dynamic range. But at the same time it allows to sample signals with high frequency components. It also has a relative high bandwidth which makes it suitable for sampling RF signals directly by means of undersampling techniques.

16 bits @ 105 MSPS: The second ADC module has a bigger dynamic range (higher resolution). It is a quite suitable for sampling signals with small power levels and lower frequency components.

Analog Front-End: The analog front-end depends on the system, there are front-ends for LF, HF, and UHF that can be connected to the processor board.

C. Software Elements

1) ADC Interface: The communication between FPGA and the ADC is realized in this module. It can be easily configure for different data rates and bit widths.

2) Base Band Generator: The base band generation takes place in the FPGA. Here the digital signal is channel coded and passed through a symbol former. The base band generator delivers two signals: In-phase and Quadrature (I and Q). In this way different modulation schemes are supported. This software module can be used to generate any base band needed.

3) Receiver Digital Front-End: The digital front-end module uses an CIC (Cascade Integrator Comb) for filtering and decimating. Figure 2 shows the block diagram of the digital front-end.

Decimation: In a digital communication system the bandwidth of the received signal is typically smaller than the resulting

FLEXIBLE DEVELOPMENT AND TESTING ENVIRONMENT FOR IMPLEMENTATION OF NEW ALGORITHMS IN RFID SYSTEMS

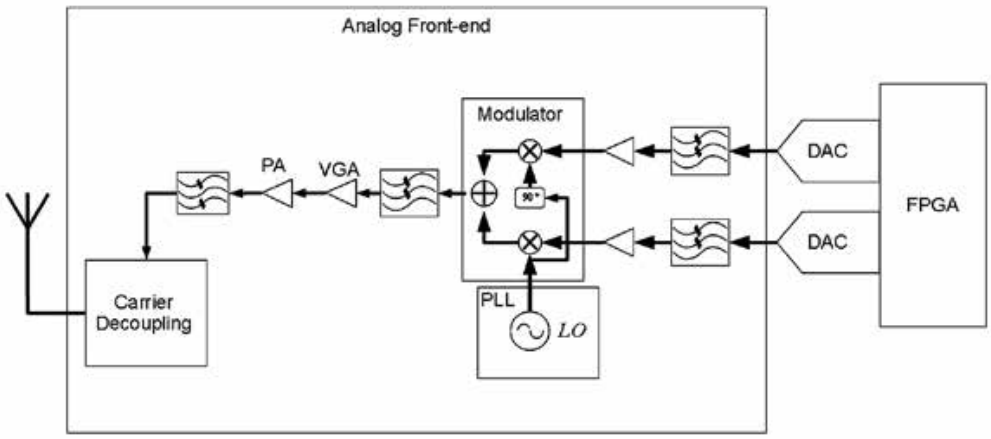

Figure 3: Block Diagram of the Transmitter

bandwidth after the sampling process. Therefore the first step on a digital receiver is a decimation block, this one re-sample the received signal with a slower sample frequency. In other words it discards a certain number of samples out of the received signal.
Demodulator: The received signal can be ASK or PSK modulated. Therefore an In-phase/Quadrature (I-Q) demodulator was programed. The IQ demodulator provides a coherent measurement of the phase and magnitud of sinusoidal signals. The IQ demodulator is the most used demodulation architecture, nevertheless other demodulation architectures can be made based on this module.
Low-pass Filter: The low-pass filter eliminates the harmonics generated by the multiplication of two sinusoids. The filter is also used for decimation; the signal bandwidth is limited by the cut frequency of the filter after the demodulator. Hence the signal can be re-sample to a quite lower frequency, relaxing the processing requirements of the further processing blocks.

4) Frequency Recovery: The I-Q demodulator is a coherent demodulator. Therefore it requires to know the frequency of the carrier signal in advance, the phase is irrelevant hence it is contained in the I and Q signals. A frequency recover element is often necessary. Here a PLL (Phase Locked Loop) is used. A PLL is basically a control loop that regulates the frequency of the oscillator until the carrier frequency is matched.

D. Characteristics

The test platform offers a flexible environment to test and implement new algorithms for RFID systems. The digital processing elements are logic modules described in software. Most of the system elements are defined with programmable logic.
Advantages:

- The digital processing elements are configurable and reusable.
- The digital processing elements can be used stand-alone or be included in a bigger system.
- New modules can be easily described and added to the system under test.
- Different receiver architectures can be tested parallel.

III. PROGRAMMING AND COMMUNICATION

This section describes how the Rapid Prototyping platform is used.

A. Module Description

The signal processing modules can be described using either VHDL or Verilog. The ISE software form Xilinx offers a complete environment for logic description. Basically any HDL generator compatible with Xilinx devices can be used.

B. Configuration

The FPGA configuration is made via the USB-JTAG port. This interface is also used for the ChipScope communication.

C. PC Interface

The test platform includes an USB-Serial module that allows to connect the Board to the PC through an USB port. At the PC this port is seen as a virtual serial port. This interface can be used to communicate with FPGA by means of a serial terminal.

D. Visualization

ChipScope: ChipScope tool inserts logic analyzer, system analyzer, and virtual I/O low-profile software cores directly into the design, allowing to view any internal signal or node, including embedded hard or soft processors. Signals are captured in the system at the speed of operation and brought out through the programming interface. Captured signals are then displayed and analyzed using the ChipScope Pro Analyzer tool [1].

Test-points: The USB-Serial port of the test board can be used to transfer data to the PC. A VHDL module allows the storage and latter transfer the data of a test point in the system. In this way test-points can be added internally in the system and visualized in the PC.

IV. DEVELOPMENT PLATFORM

In this platform many of the elements are not fixed and can be arrange as required. The board it is provided with a high performance FPGA. The resources of the FPGA are extensive and can be used to implement big systems.

The ADC can be connected to this board by means of adapter boards. An UHF transmitter has been already developed that can be connected to the Virtex 6 board.

UHF Transmitter: This module can be used in UHF RFID systems, it supports the frequency spectrum and power level specified by the standards. This transmitter is quite flexible, never the less all components are fixed, this transmitter module can be used as base for constructing other transmitters with specific capabilities. The digital interface to the FPGA board is quite flexible. Figure 3 shows a block diagram of the transmitter.

Figure 4 shows a photograph of the transmitter PCB (Printed Circuit Board). The transmitter board can be connected directly to the Virtex 6 evaluation board through a high-speed digital interface.

Figure 4: Complete Transmitter Board with FPGA Interface

Figure 5 shows a photograph of the test platform, it can be seen how the ADC and the transmitter are connected to the Virtex 6 board.

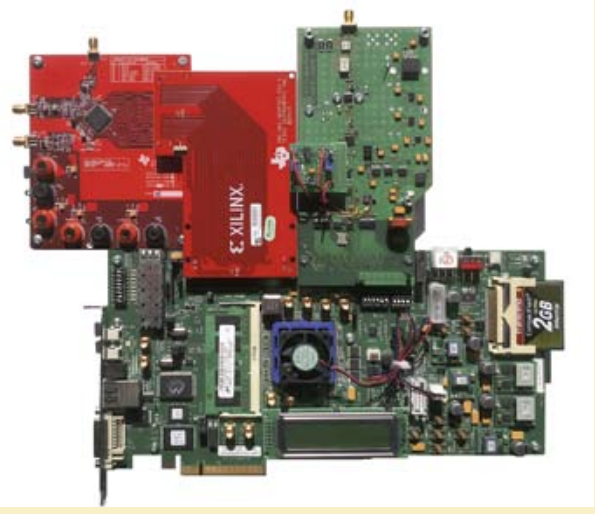

Figure 5: Picture of the Test Platform

A. Example: UHF RFID Reader

Using this platform an UHF RFID reader was developed and presented in [1]. This system is capable of readying standard

FLEXIBLE DEVELOPMENT AND TESTING ENVIRONMENT FOR IMPLEMENTATION OF NEW ALGORITHMS IN RFID SYSTEMS

tags. The protocol state machine, the radio receiver and the base band processing take place on the FPGA as well. This system has been used to test a new channel coding scheme for tag-reader communication as well. An undersampling scheme for direct digitization was implemented and test in this platform see [1].

V. PRODUCT PLATFORM

Once a system is tested and evaluated it can be implement in a smaller and low-cost platform. A digital signal processing

Figure 6: Picture of the Product-Prototyping Platform

module has been developed for special use in RFID. The module has a fast digital signal interface, a DSP specialized FPGA and a Cortex M3 micro controller. Figure 6 shows a photograph of the digital processing module. The idea is to used the digital interface to connect an application specific analog module. According to the RFID application, the analog module takes care of the signal processing task that can not be done in the digital module. The ADCs and DACs are contained in the Analog module as well.

A. Example: HF RFID System for Heart Sensors

Application specific HF RFID reader was developed, which can read pressured sensors implanted in the heart. The system is not standard compliant and requires special signal processing for the recovery of the data. The system was first developed in the development platform and then ported to the product prototyping platform. For this task an analog module was developed as well. Figure 7 shows a photograph of the system, on the right the DSP module and on the left the corresponding analog module.

Figure 7: Picture of the Heart Sensor UH-RFID Reader

VI. CONCLUSIONS AND OUTLOOK

A rapid-prototyping platform for RFID research and developed was presented. The development system has been used UHF and HF RFID systems. The system is flexible and modular, it can be used to evaluate and test new system algorithms. An product prototype for an HF RFID reader was already developed using the rapid-prototyping platform. The hardware and software modules are not limited to RFID, it could be used for other communications systems as well. [1]

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INDUCTIVELY COUPLED SENSOR SYSTEMS IN VARYING ENVIRONMENTS

R. C. Jacobi, A. Hennig

Sensor transponders are used increasingly in medicine and industry. In particular, inductively coupled systems are of interest for applications in metallic environments. A new model aims to optimize mobile devices for read-out wireless sensors. Based on outcomes smart techniques and algorithms for optimal energy transfer and signal detection can be developed. This article is an abridged and modified version based on [1].

I. INTRODUCTION

Inductive energy and data transmission is becoming more and more interesting for RFID (Radio Frequency Identification) [2], sensor transponders in medical implants [3] and wireless battery charging [4]. In most of these applications, simultaneous energy and data transmission via inductively coupled coils is necessary. In particular for the employment of mobile sensor transponder systems in industrial and medical applications, the requirements are rising. To increase the read range and efficiency, resonant circuits with a high quality factor are applied; however, these systems have to be optimized, due to the sensitivity to environmental changes.

Antennas in inductively coupled sensor transponder systems consist of coils in a resonant circuit. In the majority of these systems, the so-called load modulation is used for data transmission from the transponder to the reader. An additional load is switched on and off in the transponder depending on the data signal that is to be transmitted. The additional load causes a change of the current in the transponder coil and hence in the magnetic field strength. This can be detected in the reader device by a suitable receiver.

II. REQUIREMENTS FOR WIRELESS SENSOR SYSTEMS

The applications of inductively coupled sensor transponder systems are multifarious and differ significantly in the occurring effects. Antennas have to be designed adjusted for each need and environment. Our simulation shows how the system of coupled oscillators behaves in a potential environment. In particular, the analysis addresses the parameter range for stable communication, the carrier frequency for the best energy supply and the impact of the environment on the data communication. The input parameters for the simulation comprise the different antennas, coupling factors and environments, which exert influence on the transfer functions. As a result we find important considerations for the hardware design as well as for the signal processing of the data. The aim is to obtain smart techniques and algorithms to optimize the energy transfer and signal detection of mobile devices.

III. SIMULATION OF INDUCTIVELY COUPLED SYSTEMS

The simulation of passive sensor transponder systems needs its own approach due to the special system setup. In full-duplex mode (FDX), the reader sends a magnetic field to supply the transponder with energy even when the transponder is sending data. The change of the signal at the reader front-end, i.e. the modulation degree, is quite small.

A. Potential Effects in Varying Environments

In the design process of a sensor transponder system, it is important to understand which influences create the observed effects. The major advantage of a simulation is to be able to vary the parameters selectively.

1) Effects of Environmental Materials

a) Detuning of Resonant Circuit

In a magnetically neutral environment or for constant permeability, the magnetic flux Φ is proportional to the current [5]. The proportionality factor is in accordance with the inductance L [5]. Hence changes of the resulting magnetic flux Φ due to e. g. eddy currents involve a change of the equivalent inductance L'. The resonant circuit detunes.

b) Losses

Every real coil has a serial resistance. In presence of e.g. eddy currents, due to metal in the environment, the equivalent serial resistance of a coil increases.

INDUCTIVELY COUPLED SENSOR SYSTEMS IN VARYING ENVIRONMENTS

2) Coupling of Oscillators

Even if two inductively coupled resonant circuits have equal natural frequencies $\omega_1 = \omega_2 = \omega_0$ the frequencies where the resonant circuits exchange energy and hence allow the system to resonate are given in [6] as

$$\omega' = \frac{\omega_0}{\sqrt{1+k}} \quad \text{and} \quad \omega'' = \frac{\omega_0}{\sqrt{1-k}} \quad (2)$$

where k is the coefficient of coupling. Hence two maxima in the transfer function can be an effect of two different resonance frequencies of the respective circuits or an effect of high coupling. The impact on transponder systems is shown in Section IV.

B. Implementation in Matlab/Simulink®

In order to realize a simulation model with the required flexibility, the simulation is implemented in Simulink®, controlled by a Matlab® script. The transponder system can be described by a system consisting of three transfer functions H_e for the energy transfer to the transponder, H_d for the data transfer and H_s for the superposition of the carrier to the receiver tap. Derived from the equivalent circuit, a model containing differential equations can be obtained.

IV. EXPERIMENTAL SETUP AND RESULTS

To verify the model in practice, the energy transfer function H_e shall be investigated under the influence of a high coupling factor, i.e. a high mutual inductance. The experimental rig includes two ferrite rod antennas aligned on one axis – one applied as a transponder coil and one applied as a reader coil.

The inductances and serial resistances of the antenna coils are obtained by a measurement. The capacitors are chosen to tune the resonant circuits to the same resonant frequency 127 kHz. The accordant input and output of the energy transfer function is connected to a network analyzer. Fig. 1 shows the comparison of the measurement and the Simulink® simulation. With decreasing distance of the coils, the coupling increases. The transfer function shows two maxima at high coupling corresponding to a small distance. This behavior, described above in Section III, causes a damping at the primary resonant frequency. The two resonances are identifiable in the simulation as well as in the measurement for a high coupling. Caused by the ferrite rods, a further influence has to be taken into account. Due to the ferrite of the respective other coil, the resonant circuits are slightly detuned to a lower frequency at small distances.

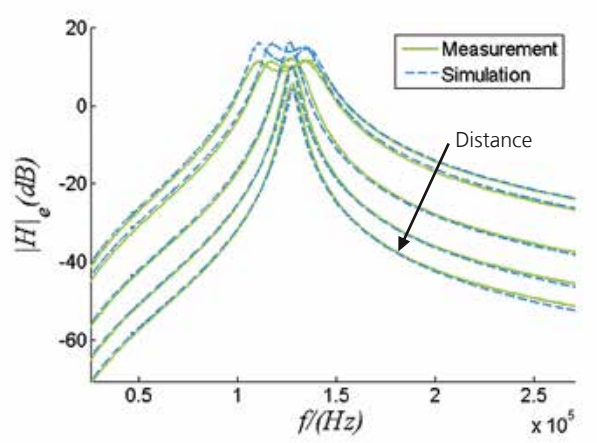

Figure 1: Energy transfer function H_e, simulated and measured, at five distances (2 mm, 4 mm, 20 mm, 40 mm, 60 mm) with respective mutual inductances [1]

V. CONCLUSIONS AND FUTURE WORK

The model enables realistic simulations regarding the impact of detuning, losses and coupling effects. This leads to the detailed understanding necessary for optimum performance of future developments. The result of the simulation is verified by comparison with a measured transfer function.

Further analyses and comparisons will be performed to design advanced reader techniques. An approach for designing such a smart reader core module is given in [7]. Based on the resultant design considerations, adaptive algorithms for energy supply and adaptive signal processing for data transmission will be developed to cope e.g. with low signal-to-carrier-ratio, low signal-to-noise-ratio and linear distortions.

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ENHANCED ENERGY SUPPLY FOR SENSOR TRANSPONDERS IN METALLIC ENVIRONMENTS

R. C. Jacobi, G. vom Bögel, A. Grabmaier

Low frequency transponder systems are the method of choice in metallic and hydrous environments. Metal in e.g. industrial and medical environments has a significant influence on these systems. An analysis of the influences of metal on the reader circuit impedance and the energy transfer function is presented. A smart approach to compensate the detuning of resonant circuits in mobile devices is given. Finally applications in metallic environments from the current research are presented. This article is an abridged and modified version based on [1].

1. Introduction

Low frequency (LF) transponder technology is applied in access control and animal identification marking. In a lot of medical and industrial applications it is the method of choice, on account of its robustness in metallic and hydrous environments.
This article is focussed on mobile reader devices used in metallic environments.

Passive transponders are needed wherever the use of a battery is costly or hardly possible, e.g. for medical implants. These devices need to be supplied solely by the reader's field. RFID applications and applications for passive transponders which not only transmit an identification number are a matter of interest. In particular the power consumption of sensor transponders presents a high challenge in many applications.

2. Effects of Metal

Low frequency transponder systems use coils to transmit energy and data. Resonant circuits are formed with antenna coils and capacitors tuned to a dedicated carrier frequency. Due to the resonance the efficiency of energy transmission per voltage induction can be improved. The level depends on the quality factor of the resonant circuits – basically on the quality factor of the antenna coils. However, a high quality factor causes different problems. Due to the small bandwidth the transfer function drops quickly next to the resonance. Thus the transponder energy supply depends on optimal tuning. Tuning of resonant antenna circuits is usually executed in a neutral environment such as air. Deploying the transponder system in e.g. a metallic environment detunes the antenna circuits as described subsequently. In the majority of LF reader designs the quality factor is reduced to achieve a stable operation and avoid heavy influences of the environment.

2.1 Influences on the Transfer Function

Low frequency systems are quite well deployable in metallic environments compared to techniques in other frequency bands. Though, metal influences the transfer function of the transponder's energy supply, in particular in systems with a high quality factor. The inductance L is defined in [2] as the proportionality factor between the magnetic flux Φ_g and the generating current i:

$$\Phi_g = L \cdot i.$$

Metal influences the resulting magnetic flux Φ_g and causes in the majority of cases a decreasing of the equivalent inductance of the coil and an increasing of the equivalent serial resistance due to eddy currents.

2.2 Energy Range

The energy range is defined as the maximum distance between reader and transponder coils, where a transponder is still sufficient supplied. The range is defined by the quality factors, the antenna geometries and the antenna environment, the available input and needed output energy and the frequency tuning.

The disadvantage of a reduced quality factor is a reduced energy range. To enhance the energy range or rather the quality factor any additional resistors are omitted in the resonant circuit of the reader. Additionally an advanced antenna design may enhance the energy range significantly.

Environment changes with each application, each transponder as well as each position of the reader during the reading operation. On this account the optimization is focussed on the reader side.

The detuning caused by the change of the inductance can be compensated for a defined environment with an adapted tuning capacitance. Hence it is possible to tune the transponder antenna for a fixed position; however, the tuning of the reader antenna is more difficult. Especially in harsh environments a solid encapsulation as a screw for sensors is needed. The subsequent simulations present the influence of such metallic sensor encapsulation on typical reader resonant circuits with different quality factors.

Approximating the antenna coil to the screw detuning takes place. Furthermore the quality factor of the coil and hence of the resonant circuit decreases due to eddy current losses.

2.2.1 Simplified Equivalent Circuit for SPICE Simulation

As described in [3] a LF transponder system can be described with a transformer equivalent circuit.

To demonstrate the effects occurring in metal environments a simplified equivalent circuit is implemented in the circuit simulator LTspice© from Linear Technology (Figure 1). The resonant antenna circuits consist of C_R, R_R and L_R for the reader and C_T, R_T and L_T for the transponder respectively. $L_{R,T}$ and $R_{R,T}$ are the inductance and the resistance of the real antenna coil, $C_{R,T}$ is the tuning capacitance. R_C denotes the real part of the chip impedance. The mutual inductance M defines how much energy can interchange between the two resonant antenna circuits.

V_R denotes the reader source voltage, V_T denotes the voltage at the resonant circuit of the transponder and the receiver voltage V_{Rec} is here tapped across the capacitor C_R.

2.2.1.1 Simulation of the Transponder System

To consider the energy transfer to transponder the mutual

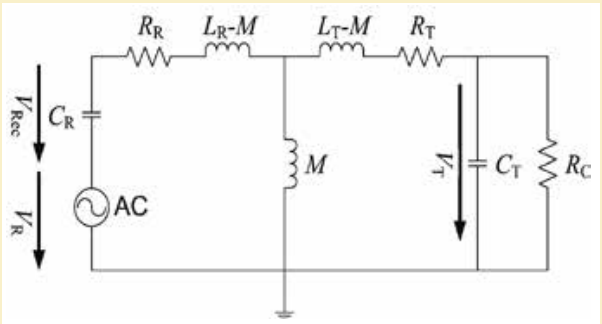

Figure 1: Simplified equivalent circuit of a transponder system for simulations in LTspice©, [1] modified

inductance M is set to a fixed small value for the following simulations in LTspice©. This fixed setting extracts the influence of the metal on the transfer function.

The equivalent parameters of an antenna coil are measured at 125 kHz. The equivalent inductance and serial resistance are determined without the screw and flush with the screw. The

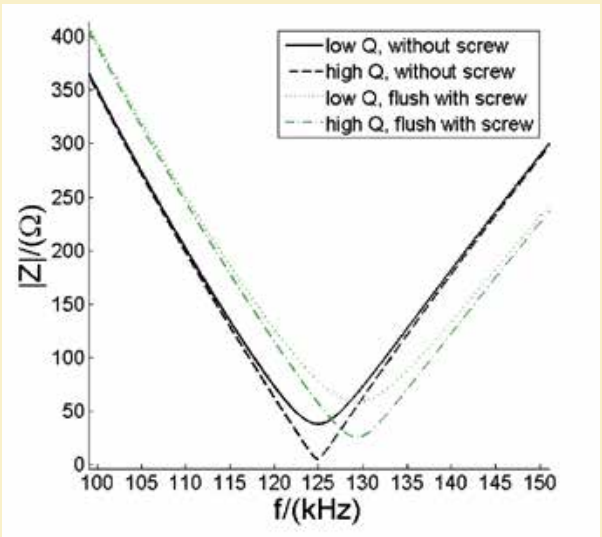

Figure 2: Impedance simulations (absolute value) of the resonant reader circuit with a coupled transponder circuit [1]

ENHANCED ENERGY SUPPLY FOR SENSOR TRANSPONDERS IN METALLIC ENVIRONMENTS

capacitor C_R is selected to tune the resonant circuit to 125 kHz without the screw. The simulations are performed with a reduced quality factor (low Q) and without an additional serial resistor (high Q). In the simulation for a high quality factor circuit the serial resistor R_R consists only of the measured equivalent resistance of the coil. The impedance of the reader antenna circuit is computed in Matlab® with the imported LTspice© simulation data.

Figure 2 shows the reader impedance with the coupled transponder circuit. The resonance frequency of the reader antenna circuits depends on the equivalent inductance L_R. The quality factor Q defines the minimum value for the impedance. In this example the frequency in the minimum is as expected for the impedance without the screw at 125 kHz and for the impedance affected by metal for both Q values at 129 kHz.

In contrast to the impedance, in the transfer function from reader to transponder the frequency of the maximum depends as well on the quality factor Q. The transfer functions specify the transmission of voltage from the reader source (V_R) to the transponder resonant circuit (V_T) for the four cases described before. The transfer functions calculated in Matlab® by the imported LTspice© data are shown in Figure 3. The frequencies of the maxima in the simulations without metal persist at 125 kHz whereas the maxima in the simulations of the transfer function affected by metal are located at approx. 127 kHz and approx. 129 kHz, depending on Q.

3. Optimization of Energy Transfer

To enhance the energy range the system may be optimized by an optimum carrier frequency. A feasible solution generating a frequency tuned on the reader antenna is a loop gain oscillator. For the implementation of such adaptable systems control circuits for stability are needed. Moreover the carrier frequency is adapted to the resonance frequency of the reader antenna impedance [4]. Depending on the quality factor this frequency may differ significantly from the optimum frequency for energy transmission (Figure 3).

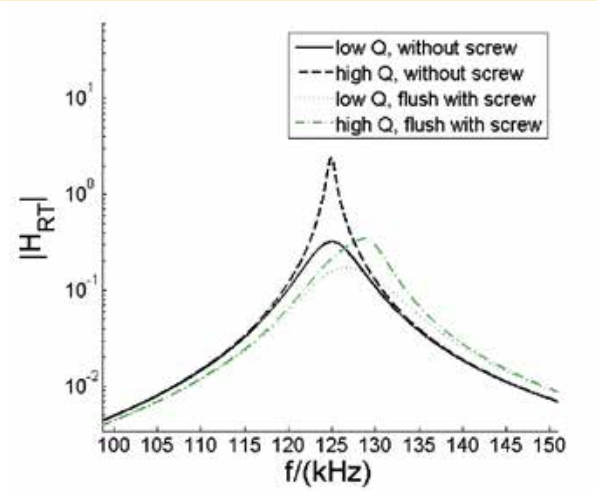

Figure 3: Simulation of the transfer function from reader voltage V_R to transponder voltage V_T [1]

An alternative for a tuned antenna circuit is a variable tuning capacitance. In automatic systems it is realised with an array of switchable capacitors which compensate the detuning caused by a changing in the inductance in a limited range. Due to the needed electric strength of the capacitors the dimensions of such an array are large compared to the other electronics. This solution is an expensive and not suitable approach for mobile systems.

3.1 Approach for a Smart Reader Core Module

The presented approach for mobile reader devices is the extensive reduction of analogue hardware and a variable applicability for different requirements and environments.

Complying with these requests a class D amplifier, which deliver the needed energy efficiency for mobile devices, is deployed. Above all it can be actuated by an easy square wave signal. Hence a separately excited power amplifier can be realised.

A system with a serial resonant circuit at the reader and a parallel resonant circuit at the transponder is employed. A

schematically drawn equivalent circuit of the system is shown in Figure 4. C_1 and C_2 constitute a capacitive voltage divider for the receiver tapping. The resistor R_{MOD} denotes the switchable resistor for the load modulation.

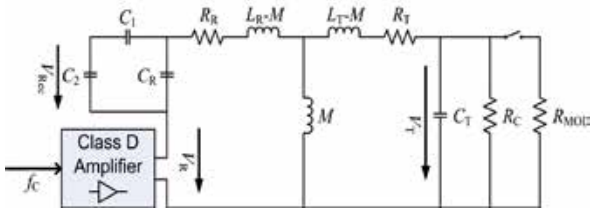

Figure 4: Schematic equivalent circuit of a transponder system for a mobile reader device, [1] modified

The presented hardware front-end allows the adaption of the carrier frequency to enhance the energy range in e.g. metallic environments. The implementation performs with a digital controlled analogue front-end. An algorithm may find the optimum carrier frequency for energy and data transmission depending on different factors, as the antenna quality factor or the detuning. Hence the reader core module copes with different antennas. In this approach the wide scope of digital signal processing can be applied to optimize the communication whereas the hardware is minimized.

4. Applications

In the following further applications in metallic environments from two different scopes are presented.

4.1 Pressure Sensor Transponder for Quality Control of Vacuum Insulation Panel

The pressure inside a vacuum insulation panel (VIP) is an important indicator for thermal insulation properties. A passive sensor transponder developed at Fraunhofer IMS fulfils the function of contactless measurement of pressure and temperature through covering metal layers and presents the best opportunity of quality assurance [5]. The sensor transponder consists of a fully integrated microelectronic circuit and an antenna, both mounted on a printed circuit board. Measurements are taken with a mobile reader unit.
Figure 5 shows the handling while taking current pressure and temperature values.

Figure 5: Readout of the inside pressure and temperature of a VIP [1]

For the direct measurement of pressure and temperature inside the panel the sensor has to be placed inside the enclosure. The actual size of the sensor transponder is about four millimetres in thickness and about 25 millimetres in diameter. So it is advised to form a cavity of this size into the VIPs core board and to insert the sensor transponder in this place. This establishes a fixed mounting position and avoids shifting during handling and evacuation process.

The wireless transmission can even be achieved through the gas-tight enclosure including a thin metallic coating.

4.2 Medical Implants

Medical implants have to fulfil highest requirements regarding reliability. Where sensors or actors do not need a continuous activity, but activities are initiated occasionally from outside

the body, like monitoring of blood pressure once a day, it's a good choice to use the principle of sensor transponders [6]. Basically the amount of toxic materials is the lowest, because there is no battery inside the implant. Additionally this leads to the fact that no battery change for the implants is needed.

The biocompatibility is a key-issue for long term abidance inside the body. Titanium is known as material best suited for the encapsulation of medical implants. An additional advantage is the impermeability to liquids.

However, handling the influence of titanium on the transmission of energy and data is difficult. Using a titanium encapsulation modifies the transfer function as described in chapter 2. Fraunhofer IMS has developed the electronics of a medical implant as well as a reader unit. The implant electronic has the capability to measure pressure and temperature at a high sampling rate. The implant is capsulated in a hermetic closed Titanium housing. A pressure measure is implemented by transferring the pressure from a Titanium membrane to the on-chip pressure sensor.

5. Conclusions

Low frequency transponder systems are the method of choice for many special purposes regarding applications in hydrous and metallic environments. The transfer function of the channel for energy transmission is strongly varying with the environment. The scale of different influences is estimated. It is shown that the transfer function depends on e. g. the quality factor and the interaction with materials in the environment. An approach for a smart reader core module is given to cope with these challenges.

5.1 Future Work

An advanced simulation is implemented in Matlab/Simulink® [7]. Further effects in LF transponder systems with different quality factors are under examination. The consequential conclusions will be integrated in an algorithm implemented in a test setup with a digital controlled analogue front-end.

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PSEUDORANDOM NOISE BASED CHANNEL CODING SCHEME FOR TAG TO READER COMMUNICATION IN UHF-RFID SYSTEMS

S. Grey, G. vom Bögel, A. Hennig, A. Grabmaier

This paper presents the capabilities of using Pseudorandom noise (PN) codes as a channel-coding scheme for the tag to reader communication. A comparative of the standardized coding scheme and the PN is presented. This coding scheme will be compared to the EPCglobal GEN 2 standardized Miller codes in order to establish its advantages and disadvantages.

1. Introduction

The use of Ultra High Frequencies (UHF) for RFID Systems has grown considerately in the recent years. The implementation of the radio identification in the logistics and commercial applications, as well as the standardization by the EPCglobal [1], have opened the doors for a wide range of practical applications of the RFID technology. The channel characteristics, the frequency tolerances in the tags, and the requirements for multi-functionality for various frequencies/standards, increase the challenges for the RFID-readers. In the exploring of new ideas and system improvements, some results lead to changes that are not complies with the standards. Nevertheless important improvements can be archived even though it may lead to no standardized systems.

2. Channel Coding in UHF RFID

This paper is referred to the EPCglobal Gen 2 standard and the system description given in it. According to this standard the tag to the reader communication takes place using backscatting modulation techniques. The information is encoded in 4 possible forms FM0, Miller 2, Miller 4 or Miller 8 see Figure 1.

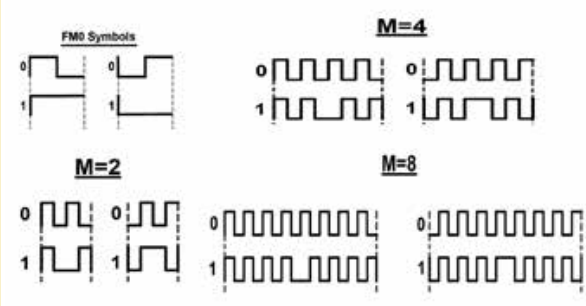

Figure 1: EPCglobal GEN 2 Channel Coding Scheme for Tag to Reader Communication

The reader requests the information from the transponder and specifies the data rate as well as the coding scheme to be used. There are some characteristics referring to this coding scheme: the FM0 coding is the base for the other three types. The Miller 2 to Miller 8 can be seen as a combination of FM0 symbols. The FM0 symbols are orthogonal to each other, but the Miller 2 to Miller 8 symbols are not. Due to its non-orthogonality, the cross correlation of the Miller symbols does not result in a maximum euclidean distance.

The concept of these long symbols representing a single one or zero is sub-optimal. Another coding scheme can be used that takes advantage of orthogonality and the correlation gain.

3. Pseudorandom Noise based Channel Coding in UHF RFID

A pseudorandom noise (PN) sequence is a signal with similar characteristics to noise, it satisfies one or more of the noise statistical randomness.
It was decided to use gold sequences for test and implementation purposes. Gold sequences are binary sequences of length 2^(n-1) with a small cross correlation between sequences. This makes them convenient for digital signal transmissions. But other PN sequences can be used as well. Sequences of different lengths were tested and compared against the standardized coding scheme, the results would be shown in section 6.

The orthogonality of the gold sequences increases with rising length. Short lengths present little or none orthogonality, therefore in order to demonstrate its feasibility for RFID systems, a set of sequences of 31 length was used. For a digital representation the next possible power of 2 is 16. Using 16 different sequences 4 information bits can be transmitted by one single symbol.

4. Simulation

In order to analyze the characteristics of the coding schemes, a simulation of the entire system was done using Matlab [9].

4.1 Bit-Error-Rate Test

The simulation was done for the EPCglobal Gen2 coding scheme and for the gold sequences. The length of the used Gold sequences were chosen as follow:

- gold sequence length 3 as a substitute for Miller 2
- gold sequence length 7 as a substitute for Miller 4
- gold sequence length 15 as a substitute for Miller 8

In this way the symbol lengths of the Gold sequences are comparable to the Miller symbols; considering the half of an FM0 code as a chip. Two Gold sequences for each substitute are used, one to represent a "1" and the other a "0". To measure the bit-error-rate (BER) 100 000 bits were sent for each encoding scheme and at different SNR values. The SNR is set by simply increasing the added noise. The graphic in Figure 2 shows the resulting BER of the received signals according to its SNR. It is important to note that the chip length was normalized to one half of the time period of the FM0 symbol. Therefore the band width of all coding symbols is the same, only the symbol length changes. In this way the performance of each symbol form can be compared to the performance of the others.

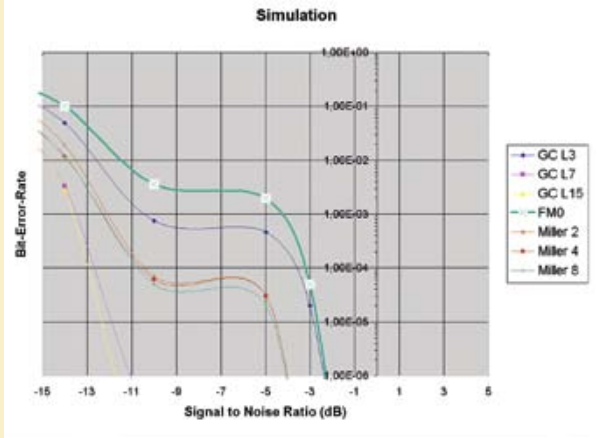

Figure 2: BER Results of the Simulation

The Figure shows the results of the simulation. It can be seen that the BER is reduced as the length of the miller codes increases. The correlation with a longer symbol increments the SNR of the signal reducing the BER [8]. The big difference between the Miller codes and the gold sequences of length 7 and 15 is also significant. The gold encoded signals present a quite better BER compared to their corresponding Miller symbols of the same length.

5. Hardware Implementation

5.1 Bit-Error-Rate Test

After showing the possible advantages of the gold sequences as a coding scheme in UHF RFID systems, the results were corroborated by implementing the system in our rapid prototyping platform. The bit-error-rate test was repeated under the same conditions as for the simulation. 8 random bits are generated in matlab, these ones are transferred to the FPGA where they are encoded. The encoded signal is used by a test transponder to switch the matching circuit of the antenna. This creates a backscatting signal that is received back by the hardware platform. Figure 3.

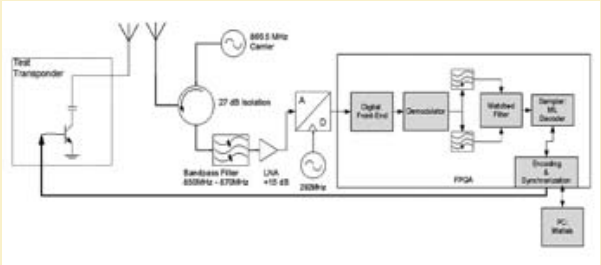

Figure 3: BER Test Block Diagram

In order to decode and recognized the symbols sent by the transponder, the base band signal is correlated with the possible

PSEUDORANDOM NOISE BASED CHANNEL CODING SCHEME FOR TAG TO READER COMMUNICATION IN UHF-RFID SYSTEMS

symbol forms. The signal is sampled at the symbol rate. The correlation that provides the maximum output value determines which symbol was sent. The received binary data is transferred back to Matlab where it is compared to the sent data in order to find possible errors in the transmission. This procedure is repeated for all the codes and at different SNR values. The SNR setting was done by changing the distance between the tag and the reader antenna. Figure 4 shows the resulting BER using different coding schemes.

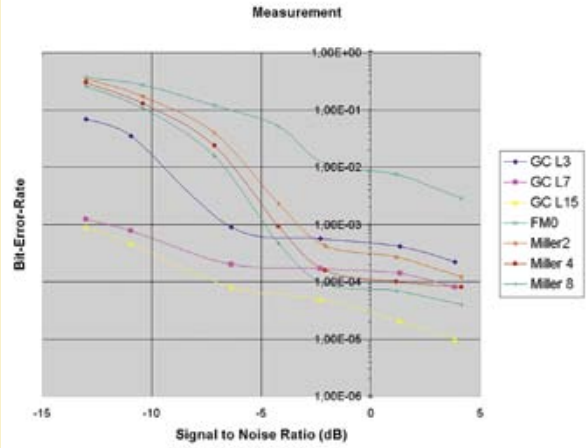

Figure 4: BER Results of the Measurement

From Figure 4 it can be seen that the performance of the Miller coding scheme is worse than it was shown at the simulation. By the PN coding scheme the BER does not converge to zero as fast as by the simulation. Important is the notorious difference between Miller and PN codes, the real system even shows a bigger difference than the simulation. The unexpected straightening of the curves at higher SNR values could be caused by bit errors that are introduced by the hardware and the imperfections in the implementation.

Even though the simulation was made as close as possible to the implementation, there are some differences between the measured and simulated results. Important is the demonstration of the advantages of using gold sequences to encode information over the usage of RFID standardized codes.

5.2 Orthogonality Test

As already mentioned, the orthogonality of the gold sequences could be used to increment the data rate by sending more than one bit per symbol.

The same hardware platform was used to test the advantages of orthogonality. A random binary message was encoded with 16 possible symbol forms and sent to the test transponder. In order to decode and recognize the symbols sent by the transponder, the reader needs to correlate the received signal with all possible symbol forms. To test the coding scheme a message of 64 bits was sent, i. e. 16 symbols.

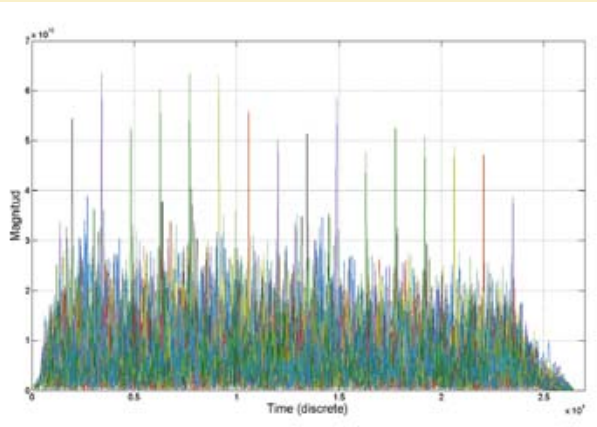

Figure 5: Correlation Bank Output

Figure 5 shows the output of the 16 correlation filters each one plotted in a different color to facilitate the recognition of each symbol. Each peak represents the detection of a respective symbol. Only one peak is seen at the sample time.

6. Comparison

It is important to point out that the comparative is relative, it only compares the performances of the coding schemes to

one another. All possible system influences are equal to all tests, which leaves only the SNR of the signal and the BER. This applies for both the simulation and the implementation. It was shown that the gold encoded messages were received with less errors than the Miller-coded ones. This is due to the orthogonality of the symbols as well as the characteristics of the PN codes, that make them less susceptible to environment influences.

The code form itself presents direct advantages, the symbols are orthogonal to one another which decreases the biterrorrate.

7. Conclusion and Outlook

This procedure can be added or be the base of new standards that could improve UHF RFID systems. The application of this concept is useful specially in high-noise environments where the distortions are considerable. The main changes to be considered are: the encoding of the digital data in the tag and the receiver architecture of the reader.

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OPERATION OPTIMIZATION FOR COMBINED HEAT AND POWER SYSTEMS

M. Walter

The cogeneration of heat and electric power with CHP (combined heat and power) systems is known as an energy efficient solution. It should be established in any case where heat or electricity is currently generated from fossil fuels. Residential and small commercial buildings offer a new field of application with great potential considering that recently more and more micro-CHP systems are available in the market. Additionally to the fact that CHP technology is not known to all relevant customers, the dissemination is hindered by the costs, since in some cases the CHP operation is not economical when using the common heat demand prioritization.

The goal of further development has to be an improvement of the cost situation. Although investment costs might not fall before reaching higher production quantities, the total costs can be lowered even now by optimizing the system operation. One starting point is the fact that the savings for locally used energy are higher than the earnings for feeding electricity to the grid. Therefore, a clever CHP device operation lowers the energy costs for the owner.

Additionally, in the near future the changes in the electricity grid will show consequences. Due to the higher percentage of renewable energies more electric energy will have to be transported, combined with high fluctuation of the grid load. Local electricity generation can lower the amount of energy to be transported and a well-controlled load balancing reduces the mentioned fluctuation as well as the peak load. These goals can be met by integration of micro-CHP sites into the so-called "smart grid", controlled either directly by the electricity provider or indirectly via variations of the energy prices.

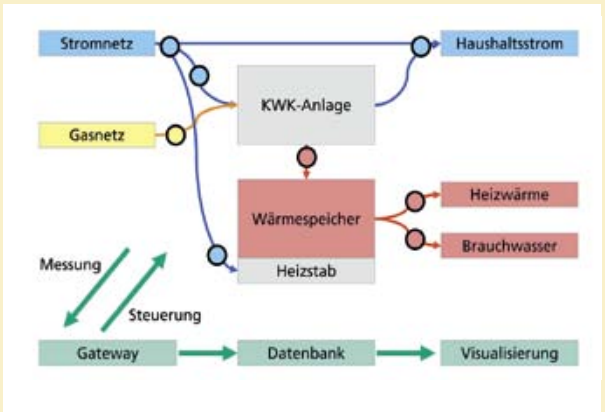
The Fraunhofer Institute for Microelectronic Circuits and Systems (IMS) is co-operating with *RWE Effizienz GmbH* in the micro-CHP research sector. The joint development of the micro-CHP product "RWE HomePower" focuses on the optimization of operation strategies, followed by the realization of the smart grid integration of micro-CHP.

For the development process a test system was set up in the research building "inHaus2" of the Fraunhofer inHaus Center. Its main component is an "ecoPOWER 4.7" micro-CHP device. This delivers up to 4.7 kW of electric power and 12.5 kW of thermal power from a natural gas engine. It can work at different power levels. With ideal settings the degree of efficiency reaches 90 %. The produced heat is stored in a heat buffer of 850 l. For research purposes it also contains two electric heating rods (9 kW of thermal power each) which can load the buffer.

The research building "inHaus2" not only provides space for the micro-CHP system but is also used as a heat sink in the test platform. The heating system can draw defined amounts of heat from the CHP heat buffer to emulate the heat consumption of an arbitrary building. The main aim is to reproduce the exact heat demand cycle of a residential home to test different CHP control algorithms under realistic conditions. The heating capacity of the inHaus2 is sufficient at any time of the year so that the tests are not limited to the winter period.

In the test setup all relevant energy flows are recorded with measuring equipment. This includes the produced and the consumed heat as well as the gas consumption and the electric flows between the electricity grid, the CHP system and the household. For both the measurement data collection and consolidation and for control purposes a gateway was developed. It combines several communication interfaces to the local environment and to the smart grid. For data gathering and the analysis of test parameters and results a database on a separate server is used.

As mentioned above, the starting point for optimization of the CHP operation is to maximize the ratio of electricity consumed compared to the total electricity production. This can be achieved if the CHP system provides exactly the amount of electricity needed. Therefore the first step is a prediction of the electricity and heat demand using statistical energy data and weather information.



Since current system concepts do not include batteries, electricity has to be produced on time. Heat, however, can be produced some hours earlier and stored in the heat buffer. This separation of electricity and heat production has the potential of adjusting both to the actual consumption. Ideally no electricity should be transferred from or to the grid while meeting the complete heat demand of the building.

However, in reality, meeting the electricity consumption perfectly is not possible, partly because the energy demand prediction will not match the actual values exactly, partly because technical conditions limit the system operation. For example, the CHP engine has minimum and maximum power levels and the heat buffer is restricted in capacity as well as having some loss.

With the introduction of time-variant electricity tariffs the complexity rises to an even higher level because the current energy price has to be included into the calculations.

Some of the shown solutions were implemented by *RWE Effizienz GmbH* in their "HomePower Mikro-KWK" product. This consists of an "ecoPOWER" CHP system extended to form a comfortable all-in-one solution. Two business models are offered. In one case the customer can buy the system and hand the operation over to RWE, the second possibility is that RWE is owner and operator of the system at the same time.

For both solutions *RWE Effizienz GmbH* optimizes the CHP system operation to improve the economic efficiency by clever measurement and control, also caring for installation and maintenance. RWE then provides electricity and heat to the customer for defined prices per kWh. Produced energy that is used in the household is rewarded with a bonus. Energy data and system status can be monitored via a web interface with visualization.

One of the next steps is the integration of micro-CHP into a smart grid. For such applications, e.g. as a virtual power plant, secure and extensible communication standards will be needed. Also inside a building local optimization potential can be found. A well-managed combination of CHP with PV or other technologies can further improve the efficient energy supply for the home. With decreasing investment prices, electricity

OPERATION OPTIMIZATION FOR COMBINED HEAT AND POWER SYSTEMS

storage is more and more likely to help with the optimization, too.

Generally, a holistic energy management approach considering all systems of the building is necessary to maximize the energy efficiency. This includes a unified communication system for measurement and control as well as sophisticated algorithms. In addition to decreasing production, installation and maintenance costs complete technology packages are required. Together with the better cost efficiency by clever system operation that should help to further establish CHP in the market.

SAMDY – TECHNOLOGIES TO SUPPORT "CARE ON DEMAND"

M. Munstermann

Introduction

The number of people in Europe age 65 and over will rise from 75 million in 2004 to 133 million in 2050 [1]. Their cognitive skills will undergo a negative change over time. This can begin with incidents like forgetting to take one's medicine and possibly end in an abnormal state (e.g., dementia or Alzheimer's disease [AD]).

In Germany roughly 69 % (as of 2009) of all patients receiving professional care can be treated in their own homes. The remaining 31 % are either partly-through day care-or completely institutionalized. Either way, the reason they are receiving professional care is that an independent authority states they are considerably limited in the activities of daily living (ADLs).

While Hong *et al.* [2] utilize an ontology-based approach, we define ADLs using task models. Our choice of task models as a definition language was driven by the concept of involving caregivers during the system design phase. This approach will strictly distinguish between impersonalized knowledge during context generation and personalized knowledge for anomalous behaviour discovery.

Changes in behaviour concerning ADLs can be seen as an early indicator of autonomy loss [3]. One of the earliest assessments of human behaviour related to the ability to live independently was conducted by Katz *et al.* [4]. A significant drawback of questionnaires such as those used in that study is that elderly people tend to lie about their difficulties (due either to fear of the consequences or to shame).

Telemonitoring products concentrate on well-being at the *health* [5] level (e.g., 24-hour ECG monitoring). We tackle the automatic detection of behavioural competence at the *functional health* level. Basically, we focus on the physical (sometimes called basic) and instrumental aspects of ADLs.

To a certain degree, people reveal their current context (activity, location, identity and time) [6] by interacting with their environment (e.g., by opening the doors of a cupboard). Assuming additional semantic information is provided, it is possible to draw inferences about any activity currently being performed simply by augmenting their surroundings with the appropriate sensors.

When considering an individual's daily habits, some repetitive patterns can easily be observed, starting with the person's wake-up routine [7]. After collecting enough context information about a specific person to create a temporal relationship model of his/her daily activities, we can assess to what extent the current day's pattern of activities matches those of previously observed days.

The SAMDY system is intended as an aid to the caregiver. To this end, we have created a novel system to support "care on demand" at different levels: during the specification phase, a clear and easy-to-understand language had to be chosen so the developer can profit from the domain knowledge of the caregiver. When it comes to visualization, we had to find a highly condensed behavioural information representation of the client's daily living skills.

Let us assume the caregiver arrives at the home of one of his clients. He has not seen that person for almost 24 hours and does not know what has actually happened in that time. Ideally, the client will report on any problems he has faced during the caregiver's absence. However, sometimes-as with the questionnaires-clients might lie or simply neglect to inform the caregiver about relevant issues.

This is where SAMDY can help the caregiver. The metric value SAMDY will generate can give an indication in terms of how normal the previous day was. When the caregiver perceives a low metric value, he/she will automatically know that something was unusual.

By comparing the previous day to the typical behaviour of that specific client, the caregiver can also find out when and where

things diverged from the norm. The caregiver can then use this information to discuss the findings with his client.

System Overview

SAMDY consists of two main building blocks: *context generation* and *behaviour discovery*, which will be considered in the following sections.

The *context generation* module will interpret events coming from the sensors and output the corresponding activities performed (ADLs). To define those activities, the system uses a model-driven, top-down approach. By first defining ADLs using models, we can then execute a conformance check in real-time. There is no need for supervised and often tedious manual labelling of datasets.

The second main module, *behaviour discovery*, will use this contextual information as input. By observing daily habits, SAMDY will construct the typical schedule of activities for a specific person. Because human activities tend to be complex and often vary, the behaviour model is probabilistic. Using this typical behaviour of more or less probable sequences of activities as a reference, current activity sequences can then be rated in relation to previously observed patterns.

The context generation is capable of real-time operation. Each sensor data or sensor event triggers an action within that module. The behaviour discovery works on a daily cycle. After a complete day the behaviour discovery will produce/update the typical behaviour and output a metric value (see Section "Metric for Anomalous Behaviour Detection").

The reason we have chosen a daily base is rooted in the nature of the human biological rhythm. Like no other, the circadian rhythm has a great influence on our life. Similar to our vital signs, our biological clock also follows this daily cycle [8].

Our sensing approach is based on reliable detection of object use, operating primarily with binary sensors. This way a maximum of the user's privacy can be preserved, *i.e.*, especially compared to audio and video surveillance systems. The objects used to perform ADLs (e.g., using the toilet or the refrigerator) basically remain the same. Manipulating a certain object will effectively distinguish the activity performed from other activities not containing that object, thus leading to a rapid reduction of possibilities with every object manipulated.

Context Generation

The context generation module has to make sense of continuously incoming sequences of such events. By leveraging the common sense knowledge of caregivers, we have defined a set of ADLs utilizing the notation of task models. This set currently consists of the following nine activities: using the toilet, transferring, waking/sleeping, dressing, eating, washing, bathing, combing one's hair and napping. These nine activities are listed in order of significance.

The caregiver has to decide which activities are to be monitored for a specific client. Depending on the physical condition of a client, it may happen that it does not make sense to monitor all possible ADLs. Therefore the caregiver might decide to leave out certain ADLs so as to facilitate a less costly sensor installation. The "waking/sleeping" activity is mandatory since it is used to detect the beginning of a new day.

We use Paterno's Concur Task Tree (CTT) notation [9], because it has been shown to be quite intuitive to understand for both caregivers and computer scientists [10]. The reason for its intuitiveness lies in its compact and understandable representation. Nevertheless, it is very powerful and flexible when it comes to modelling temporal ordering and offers a rich set of operators.

Because CTT is a representational rather than an executable language, we had to transform the activity models into an executable equivalent. Since CTT is devoted to model concurrency and asynchronous behaviour, we chose Petri nets (PNs) as the target language.

Our transformation approach exploits the Theory of Regions [11]. The algorithm will search for typical structures (regions) within the CTT model and reproduce them in PN fashion. The reason we are using two formalisms is simple: In terms of intuitiveness, CTT outperforms PNs. On the other hand, PNs have major advantages when it comes to execution and validation. The caregiver will only interact with the CTT models of ADLs. PNs are generated automatically from the CTT models.

Each activity previously defined in a separate CTT will become a single PN. All PNs will run in parallel for the context detection. This will support concurrent occurrences of activities. The transitions of the PNs are triggered by the incoming events from the sensor middleware.

At the beginning of each day (detected using the dedicated "waking/sleeping" activity), every PN is set to its initial marking (state). As soon as a sensor event indicates that part of an ADL is taking place, the appropriate PN will experience progress.

Based initially on default values, but later using perceived knowledge, each activity (*i.e.*, its PN equivalent) has a dedicated timeout value. If the corresponding activity has not been completed by the time the timeout has been reached, the activity will be logged as "incomplete" together with information about its current state (*i.e.*, which events have already been perceived and which events were missing).

From a computational viewpoint, this approach is very resource-friendly since it is completely event-driven. Compared to activity recognition approaches based on labelled sensor data (e.g., Blanke and Schiele [12]), this is a fairly formal approach to context generation. From the caregiver's point of view, our rather strict methodology is comprehensible. Caregivers want to know exactly what their clients are able to do on their own and where they experience problems. Even if the person he/she is caring for is still responsible for himself/herself, the caregiver at least has a moral commitment and a social responsibility.

Purely probabilistic models will not support the recognition of wrong (*i.e.*, incomplete) ADL executions. Ideally, an incorrect execution of an ADL would lead to a reduced probability. Nevertheless, unless a threshold is defined, it is always possible to return the most probable activity currently being recognized.

Behaviour Discovery

Our system is based on a layered architecture. The behaviour discovery tool takes the previously extracted information to the next layer, further compressing the information.

In the course of a day, every activity recognized by the context generation module (whether complete or incomplete) will be stored in an event log. The context generation and behaviour discovery modules interface via an XML format for storing event logs called Mining eXtensible Markup Language (MXML) [13]. MXML is a common data type in the data mining domain (*i.e.*, business process mining). Using a common meta-model allows for interoperability with other approaches (for both context generation and behaviour discovery).

Process mining promises to extract new knowledge from the event log. In our case, the knowledge we are looking for is the typical daily routine (process structure) of a specific person. We evaluated several process-mining algorithms (Heuristics Miner, Fuzzy Miner, Alpha Miner and Transition System Miner) before coming to the conclusion that a configurable algorithm like the Transition System Miner (TSM) [14] best fits our needs: (i) to be able to check on process conformance and (ii) to be able to adjust the balance between under- and overfitting of the output.

TSM employs trace methodology. A *trace* is a certain sequence of activities, while running TSM generates a transition system made up of states. These states describe parts of traces up to a certain point in time (or still to come, depending on the actual setting).
TSM is configurable in five abstraction levels (maximal horizon, activity filter, number of activities, order consideration and

visible activities). TSM is able to produce a PN from the derived transition system.

Configuration of the mining algorithm is needed in order to achieve a balance between under- and overfitting of the resulting process model [14]. Our algorithm applied to determine the metric will attempt to automatically find the best fit.

By utilizing the process conformance presented by [15], we can track whether current day observations already exist in the typical behaviour seen so far. If so (*i.e.*, the sequence of activities for the current day conforms to the process model), the probability for that trace can immediately be determined by multiplying of the weights of all arcs on the path. If the opposite is true *(i.e.*, the course of the current day is atypical so far), the trace of the current day has to be merged with the typical behaviour by reapplying TSM. Afterwards, it is also possible to compute its probability.

Metric for Anomalous Behaviour Detection

Introducing the plain probability of each trace has three major disadvantages. First, the probabilities for days whose traces have different lengths (*i.e.*, the number of activities performed per day) are not comparable. This has to do with the way these probabilities are computed. Multiplying an additional probability ($p_i \in [0,1]$) can either result in the same value (if $p_i = 1$) or reduce the final probability (if $p_i < 1$). Second, the absolute value will decrease over time. This is due to the fact that the behaviour model will grow (in terms of complexity) until every variation of the person's daily routine has been detected. Finally, it is not very meaningful for the caregiver.

Because of these disadvantages, we had to come up with a different measure (metric) for how typical a given day in the life of the client can be considered. If the person "fails" in performing a particular activity, it will not be processed together with the other (completed) activities by the behaviour discovery component. Therefore, the perceived behaviour will differ from the typical behaviour and lead to a reduced probability.

The metric *m* we want to propose for this purpose takes the plain probability mentioned above and scales it using the probability of the most probable path from the behaviour model:

$$m := \frac{p_M\left(tr_{current}\right)}{p_M\left(tr_{highest}\right)} \quad (1)$$

In metric (1), $p_M(tr)$ denotes the probability of trace *tr* determined using the model *M*. While $tr_{current}$ represents the trace of the current day, $tr_{highest}$ corresponds to the trace with the highest probability. In addition to these definitions, we modified the well-known Dijkstra algorithm, which normally searches for the shortest path, to find the most probable path, thereby maximizing $p_M(tr_{highest})$.

Applying metric (1), we can rate how typical a certain daily schedule is compared to the most likely one ever perceived. Reconsidering the three disadvantages stated at the beginning of this section, we have so far overcome the second and third. Even if the structure of the model varies over time, scaling by the probability of the most probable path will guarantee that, after a while, there is no continuous reduction (because $tr_{highest}$ would also be influenced by that cause). To a caregiver, a scale from 100 % (meaning the recently considered day is absolutely typical for a specific client) to *nearly* 0 % (meaning a day like this has never been witnessed before) is very intuitive.

We have also come up with a mapping between this measure and the colours of a traffic light. Green would signalize a metric value of a "normal" day and red would stand for a relatively atypical day. Yellow would be used for anything in between (*i.e.*, near the dynamic threshold between red and green). This way we could fulfil the requirement calling for intuitiveness in terms of system usability.

Realistic Simulated Evaluation of Behaviour Discovery

To conduct an evaluation of behaviour discovery, we will assume a fully functional context generation module. Carrying out the behaviour discovery evaluation in a real world setting entails

two main risks: (i) It is very time consuming and expensive in terms of equipment; and (ii) there is no guarantee that the test persons will actually change their behaviour during the study. There is no way of proving the overall system functionality if there is no variation in behaviour.

Our approach is twofold: We collected actual sensor data coming from *five* individuals' living quarters and asked the caregivers to protocol the typical sequence of ADLs for each person over a one-week time period. We then enhanced the protocols by cross-checking their entries with the events emerging from the sensors.

Even the very first representations of these ADL behaviour patterns showed that each person has a unique daily routine-like a "behavioural" fingerprint. While some people change their routines daily, others have a special routine for every single day of the week (*i.e.*, many parallel paths).

We also found indications that there is a difference between weekday (*i.e.*, from Monday to Friday) and weekend (*i.e.*, Saturday and Sunday) behaviour. Figure 1 sums up our results in terms of typical behaviour. The path added/updated last is indicated in red. While the diagram is not intended to be readable in detail, it does show how diverse the ADL behaviour of five different people can be.

Behaviour discovery works on a daily basis. The reason for this was discussed in Section "System Overview". Every day (*i.e.*, trace) in the typical behaviour of any given individual starts with getting up in the morning and ends with going to bed.

Having generated the typical behaviour for each person (*i.e.*, P1: female, 79 years; P2: female, 87 years; P3: male, 84 years; P4: male, 75 years and P5: male, 87 years), we were able to artificially (re-)produce further daily logs. This is due to the fact that the behaviour models contain more variations than actually observed.

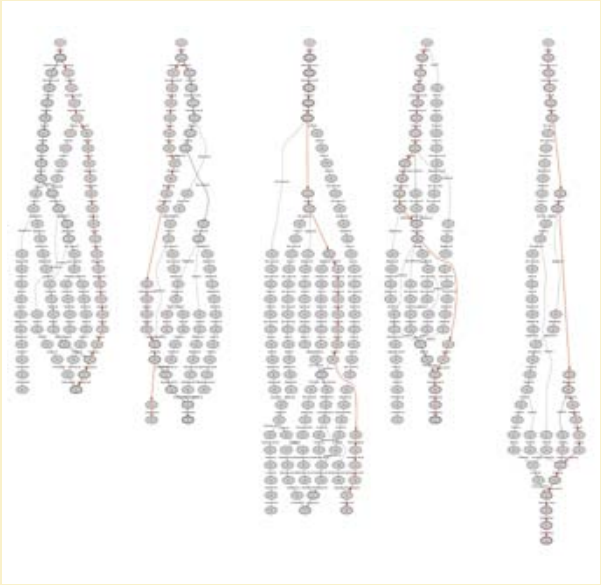


Figure 1: Typical daily behaviour in terms of ADLs of five test persons P1– P5 (from left to right)

From interviews with caregivers and the literature, e.g., [16], we know that there are four primary reasons for irregular behaviour: (i) activities can be completely forgotten (removed); (ii) they are delayed in time (delayed); (iii) they are switched with other activities (swapped) and (iv) they are performed more often than usual (repeated). The latter is the case if the person forgets that he/she has already completed a certain task (*i.e.*, retrospective memory error). This can be very dangerous if the task happens to be taking medicine.

Instead of waiting for P1– P5 to make mistakes in one of the four error classes, we artificially generated them starting with a "normal" trace. With this approach, we generated 70 days of data for each person. Every day consists of five versions: the normal one, a version with removed activities, a version with delayed activities, a version with swapped activities and a version with repeated activities. In total 350 traces were artificially generated.

The evaluation of the behaviour discovery was intended to answer the following two questions:

- For how long does SAMDY need to be installed and trained by the daily behaviour of a person before it is able to distinguish between normal and abnormal days?
- What *precision* and *recall* can the caregiver expect when relying on SAMDY?

We determined that there is a relation between the time the system has been installed and trained and the optimal threshold. This dependency can best be described by a root function. Utilizing these function characteristics as the dynamic threshold setting, we were able to answer the above-mentioned questions. Actually, both questions are closely related: *precision* and *recall* depend on the time the system is up. The longer the system is running, the higher the *precision* and *recall*. To combine both *precision* and *recall*, we chose the F_2-measure.

P5's living quarters were not equipped with sensor hardware. Consequently, we were not able to cross-check the data from the daily protocol for that individual. That is why we disregard P5 in the following discussion.

Table 1 presents the overall results regarding two different time periods. First, we calculated mean values and twofold standard deviation for the period running from two to ten weeks. Then, we compared those results to the second time period (six to ten weeks).

Table 1: Mean F_2-measure values for the denoted period applying the twofold standard deviation (values in percent)

Weeks	P1	P2	P3	P4	[P5]
2–10	98.77	96.87	99.06	98.65	94.73
	+1.23	+3.13	+0.94	+0.42	+3.21
	–2.78	–6.37	–1.76	–0.42	–3.21
6–10	99.77	98.69	99.71	98.82	95.78
	+0.23	+0.62	+0.29	+0	+2.32
	–1.04	–0.62	–1.01	–0	–2.32

Even after only two weeks, the mean F_2-measure values are better than 96.87 %. Taking the twofold standard deviation into account, this value is reduced to 90.5 %.

Waiting another month slightly improves the mean values but drastically improves the twofold standard deviation. Now, for roughly 95 % of all cases, the F_2-measure values will be better than 98.07 %, which we consider to be a quite promising result. For more details on the evaluation process, please refer to [17].

Conclusions and Future Work

We have presented a systematic approach to a system to support the caregiver called SAMDY. With our metric, it is possible to rate how typical a person's daily behaviour is when considering his/her activities of daily living (ADLs) in relation to his/her typical behaviour. SAMDY enables caregivers to take a closer look at those tasks their clients have encountered difficulties with. The corresponding activities are defined in cooperation with the caregiver using task models.

The behaviour discovery builds on the output of the context generation. After utilizing a standard exchange format, a process mining algorithm is applied. An automated balancing between under- and overfitting is performed. We received data from real smart homes equipped with sensors.

Using a dynamic threshold, we calculated that it is possible to map the metric value to the appropriate traffic light colour. Performing this evaluation in a real-life situation would have been too time-consuming. Moreover, it could not be guaranteed that subjects would actually behave in an anomalous way during observation time. Therefore, we exploited expert evaluation. Utilizing real sensor data in combination with caregiver knowledge to produce simulated sequences, we were able to evaluate the traffic light signal in time lapse.

Although our work has concentrated on detecting ADLs and finding outliers over time, the system has a generic core.

Depending on what kinds of tasks are specified (e. g., assembly line workflows), the system would also be able to identify irregularities in those tasks.

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LIST OF PUBLICATIONS AND SCIENTIFIC THESES 2012

List of Publications and Scientific Theses 2012

LIST OF PUBLICATIONS AND SCIENTIFIC THESES 2012

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Zuverlässigkeitsuntersuchungen an einem 1 µm SOI-CMOS-Prozess bei hohen Temperaturen (250 °C +).
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Einsatzgebiete und Marktpotentiale der Smart Home-Technologie.
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Scherer, K.:
Technik als Helfer im Wohnhaushalt – auch bis ins hohe Alter.
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DE 10 2011 076 046 A1

5. Theses

5.1 Dissertations

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Zuverlässigkeit von CMOS auf SOI für den Betrieb bei 250 °C.
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5.4 Bachelor Theses

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Aachen, Fachhochsch., Bachelor Thesis, 2012

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Düsseldorf, Fachhochsch., Bachelor Thesis, 2012

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6. Product Information Sheets

AVIGLE Camera
IMS-Duisburg 2012

Diagnostik braucht verlässliche Messwerte
IMS-Duisburg 2012

Lateral Drift-Field Photo-Detector for TOF-Imaging
IMS-Duisburg 2012

SPAD Performance
IMS-Duisburg 2012

Programme Inter Carnot Fraunhofer HOTMOS
IMS-Duisburg 2012

CHRONICLE 2012

Chronicle

FRAUNHOFER IMS WORKSHOP ON HIGH TEMPERATURE ELECTRONICS

From November 6th to 7th Fraunhofer IMS hosted a workshop on High Temperature Electronics to provide a forum for industry, economy and academia in this field.

HT electronics is a continuously growing market requiring new technologies, concepts and materials. Numerous applications need high temperature electronics to place circuitry in close proximity to the sensor or actor elements. In the field of oil and gas exploration as well as geothermal development high temperature electronics are already deployed in the field. In other fields of applications like automotive, industrial electronics or aerospace there is an increasing demand for high temperature electronics.

About 75 German and international representatives from industry and universities attended the workshop and used the forum for networking and exchange of experience in the field of high temperature electronics. The presentations during the workshop ranged from applications, circuits and system design, up to technologies, materials and reliability for HT applications.

A tabletop exhibition framed the event and gave insight into available products and materials. Furthermore the guests took the opportunity to participate in a guided tour through the Fraunhofer IMS wafer fab. During the evening event the participants had lively discussions and a relaxed get-together.

All in all, the workshop was a great success! Due to the good response by many participants and several inquiries for a continuation of the workshop, Fraunhofer IMS has already started to prepare the 2nd Workshop in High Temperature Electronics scheduled for 2014.

FAIRS AND EXHIBITIONS

It is a long lasting tradition at Fraunhofer IMS to participate in well-known trade fairs. These events open up new markets and bridge the gap between science and industry. Furthermore, these opportunities encourage an intensive exchange of information among our competitors and future clients. In addition these meetings strengthen existing alliances and establish new contacts.

This year we presented our latest research results and new projects at the following fairs: the Euro ID in Berlin, the Sensor + Test in Nürnberg, the "Rendez-Vous Carnot 2012" in Lyon, the SEMICON in Dresden, the RehaCare in Düsseldorf the Vision in Stuttgart and last but not least the Electronica in Munich.

The **Euro ID** is the leading fair for new trends in the field of RFID technology and applications. Fraunhofer IMS showed a new solution for the wireless measurement of pressure inside Vacuum Isolation Paneels (VIPs). VIPs are a new technology with very promising markets and revenue for the isolation of buildings or refrigerators. Another exhibit was a pressure sensor for high pressure in harsh industrial environments.

The **Sensor + Test** again attracted numerous visitors. For measurement of many biochemical substances you need beside a good sensing element a so called potentiostat to amplify very small currents and voltages. IMS has developed a fully integrated one which is easy to use, reliable, cost efficient and small. This enables customers to develop a complete new range of measurement systems for many interesting markets with high production volumes. Cameras for far infrared detection are still quite expensive because the sensor itself has to be cooled down to get good measurement results. The IRFPA sensor from IMS is the first German IRFPA sensor which is uncooled and therefore opens completely new opportunities for markets with more price pressure and larger production volumes.

For the first time Fraunhofer IMS participated in the "**Rendez-Vous Carnot**". This fair offers R&D business networking in the following sectors "Micro & Nano-Technologies", "Materials, Mechanics and Processes", Energy and Environment".

Fraunhofer IMS presented activities and and an overview in the area of process development and high temperature elec-

tronics. During two days the IMS representatives had business talks to various interesting companies, predominantly from France.

Fraunhofer IMS together with the Fraunhofer Alliance Microelectronics attended the **SEMICON** which is the leading forum for semiconductor and microelectronics manufacturing in Europe. We presented our activities in high temperature electronics and in process developments.

The **REHACARE** is a continously growing trade fair which thematizes independent and self-determined living and care at home. The business unit "Health and Care" showed innovations in bed and bath technologies which help handicaped and disabled people to live longer and safer in their own homes.

As in the years before Fraunhofer IMS took part in the **VISION fair** in Stuttgart, which focuses on machine vision technologies. It attracts numerous representatives of companies belonging to the automotive, medical and consumer sector. Fraunhofer IMS demonstrated its 3D CMOS-camera, the application specific CMOS image sensors and the outstanding uncooled far infrared sensors.

One of the IMS highlights at **Electronica** was the presentation of the high temperature electronics working at temperatures of up to 250 °C with high reliability and long lifetime. IMS has a specialized high temperature SOI process with dedicated metallization and can design complex Mixed-Signal ASICs, Sensors, µC and digital circuits including EEPROM in this process. Applications where these temperatures appear are Oil drilling, some automotive areas or Geothermic evaluation.

Beside this IMS also showed different sensor transponders for measurement of pressure, temperature, humidity and even biochemical substances like lactate.

SMART X: SOLUTIONS FOR THE FUTURE

What are the next steps for Smart Home, Smart Building and Smart City?
Retirement of Klaus Scherer, director of Fraunhofer-inHaus-Center

In April 2012 the Fraunhofer IMS and the Fraunhofer-inHaus-Center hosted a symposium on "solutions for the future through smart technical products and systems". Reknowned speakers discussed how to ensure an inexpensive and environmentally friendly power supply and how to counter the demographic change in industrial nations.

The main reason for this event was the retirement of Klaus Scherer, founder and director of the IMS departments SAT (System and Application Technologies) and IRG (Intelligent Room- and Building Systems) as well as the Fraunhofer-inHaus-Center for many years.

A retrospective section, a festive dinner and an open-end party followed the symposium. Long-term sponsors, business partners and colleagues acknowledged the great collaboration with Mr. Klaus Scherer and wished him farewell.

The Fraunhofer InHouse-Center

FUTURE IDEAS OF CMOS IMAGING IN DUISBURG

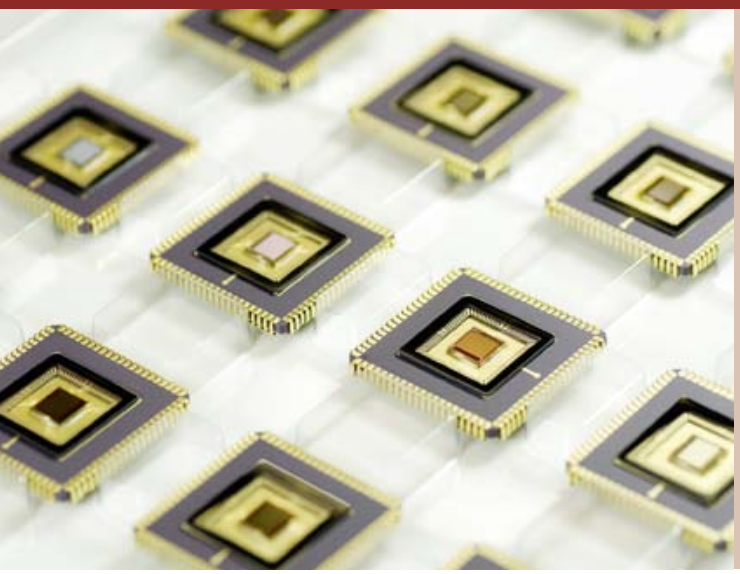
International experts working in the field of CMOS Imaging came together at the 6th Fraunhofer IMS Workshop on CMOS Imaging in Duisburg on 12th and 13th June, 2012.

Discussing new developments in 2D-imaging and 3D-time-of-flight was one of the aims of this event. Reknown speakers contributed with excellent talks to this area, to name just one is Albert Theuwissen, coming from Harvest Imaging and speaking about the effects of CMOS scaling. Interesting for the audience was also thinking about how to improve sensors and talking about applications even in the area of bolometers and x-ray. Ziv Attar, CEO of OpEra Optics gave an excellent insight on Optics for CMOS Imagers and further contributions dealt with camera testing and SPADs.

The discussion of all the presented contents was very fruitful and naturally also the networking aspect was important and estimated by the participants.

The presentations of our sponsors TriDiCam and Aspect Systems found high interest and as in the years before an exclusive event was the social meeting on the first evening which was this time in a restaurant next to the regatta course in Duisburg.

The next workshop being planned for 2014 is already in mind of the organisators. For more information about this actual programme please have a look at www.ims.fraunhofer.de in the category events.



THE OPENING OF THE ASSEMBLY LINE

The Fraunhofer IMS is one of the leading institutes in Germany for applied research and development in microelectronics and CMOS-technology and offers a wide range of services and production of in silicon based devices and systems.

After finalisation the rebuilding of the new micro-systems technology lab (MST-Lab&Fab) in 2011 the Fraunhofer IMS investigated und rebuilt in their clean rooms for the wafer level testing and assembly line in 2012.

Now the Fraunhofer IMS are able to offer their services in different clean rooms with class 100 and 1000. The clean room area of 1200 square meters allows wafer testing of 8 inch wafers, assembling of ICs in ceramic packages or as chip on board (COB), and again testing on device level.

Our services for testing and assembly from small quantities to several million units per year are:

- Full test service
- Application specific tests
- Device tests
- Test program development
- Test for pilot series
- Wafer grinding
- Wafer dicing
- Die bonding: ceramic packages, lead frames, chip on board, etc.
- Wire bonding: ceramic packages, lead frames, chip on board, etc. with Au- and Al-wire
- Encapsulation with Glob-Top or lids solder.

PRESS REVIEW

Auto-ID-Anwendungen haben den Mehrwert im Blick

Automatische Identifikation bietet nach wie vor großes Potenzial, Prozesse in Fertigung und Logistik zu optimieren. Techniken und Integrations-Know-how sind vorhanden und werden kontinuierlich weiterentwickelt. Hard- und Software sowie die Implementierung von Anwendungen haben einen hohen Reifegrad erreicht.

KONRAD BUCK

Jetzt kommt die nächste Umsetzungsphase: Auto-ID-Lösungen gehen in die Breite. Das lange postulierte „Internet der Dinge" mit vernetzten Einzelteilen, Produkten und Verfahren ist zum Greifen nahe.

Auf der Fachmesse Euro-ID 2012 in Berlin präsentieren Aussteller und Anwender die ganze Bandbreite von Produkten und Services für die automatische Identifikation von Warenbestandteilen und Produkten. Vom 24. bis 26. April 2012 stellt das Branchentreffen auf dem Berliner Messegelände die neuesten Trends bei RFID, Sensorik, 2D-Codes, Biometrie, Barcodes, mobiler Datenerfassung, RF-Kommunikation, Systemintegration und Kartentechnologie vor.

Software im Hintergrund ermöglicht den synchronisierten Datenimport. Erfasste Daten werden nutzerdefiniert weitergeleitet.

Daten mit dem Scanndy „en passant" erfassen

Die Auto-ID-Anwendung des Ausstellers Advanced Panmobil erlaubt die mobile Datenerfassung quasi im Vorübergehen. Einmal erfasste Daten gelangen per USB-Upload auf den PC. Hierfür werden einfach Scanner und Computer via USB-Port verbunden, wenige Sekunden später erscheinen die gesammelten Daten entweder direkt in Excel, Word oder einem anderen voreinstellbaren Programm. Sollen im Scanner erfasste Daten nicht zuletzt kann die Panmobil-Funktion auch E-Mails schicken, und zwar ohne dass Outlook oder andere Mailprogramme gebaden sein müssen. Damit lassen sich die erfassten Daten an einen oder auch unendlich viele Adressaten verschicken. Diese Funktion erlaubt es sogar, die Mails vorzugestellt zu layouten. Dadurch kommen Mailformulare direkt aus dem Erfassungsprozess und gelangen, nach den Layoutvorgaben des Versenders grafisch anstatt, beim Empfänger.

ti. Bücher oder Ivoder haben die Vorteile erkannt und nutzen die Panmobil-Scout-Technologie – mit kräftigen Umsatzsteigerungen und deutlichem Anwendernutzen.

Regallager checken sich selbst auf Standfestigkeit

Das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) zeigt in Berlin einen neuen Crash-Sensor für erhöhte Sicherheit in Lagerhallen. Aus Gründen der Arbeitssicherheit müssen Regale in Lagerhallen regelmäßig auf ihre Stabilität überprüft werden, wie es die Norm EN 15635

Wird ein solches Luftkissen angefahren, registriert der Sensor die dadurch verursachte Druckschwankung und meldet sie über eine Funkstrecke an eine zentrale Kontrollstation.

te kontaktbehaftete Chipkarte ist derzeit die elektronische Gesundheitskarte (EGK). Das Ausweisdokument wurde im Oktober 2011 eingeführt und trägt die Verwaltungsdaten auf einem vom BSI zertifizierten Hochsicherheits-Chip. Eine Vielzahl von Krankenkassen hat PAV – Mitentwickler des neuen Versichertenausweises – mit der Produktion der EGK beauftragt. Daneben produziert PAV kontaktlose Ausweisdokumente für Unternehmen und Institutionen, beispielsweise die Polizei von Abu Dhabi. Der Wüstenstaat setzt dabei auf besonders hitzebeständige Lösungen wie PC- oder PET-Karten. Beide Materialien weisen eine Hitzebeständigkeit von bis zu 120 °C auf. Aufgrund des robusten Materials können die Karten bis zu zehn Jahre eingesetzt werden.

Spezielle Hybridkarten verfügen über unterschiedliche Kartentechnik

Neben dem richtigen Material-Mix ist es darüber hinaus erforderlich, die Funktionen der Karten zu erweitern oder zu kombinieren. Für solche Fälle eignen sich Hybridkarten. Diese sind mit mindestens zwei unterschiedlichen Informationsträgern (Chips) ausgestattet.

Um eine besondere Hybridkarte handelt es sich, wenn das Trägermaterial zwei unterschiedliche Kartentechnologien enthält und

Sensortransponder

Passive Sensortransponder erlauben das berührungslose Erfassen von Messwerten und Identifikationsdaten etwa an schwer zugänglichen Orten oder an rotierenden Maschinenteilen und erhalten ihre Energie aus dem Anten-

nenfeld des Lesegeräts. Das Fraunhofer IMS zeigt auf seinem Stand einige Exponate für unterschiedliche Anwendun-

MM Logistik, März 2012

Design & Elektronik, März 2012

Drahtlose Fensterkontakte – wartungsfrei und energieautark

Fensterkontakte melden uns, welche Fenster im Haus offen oder geschlossen sind. Neuere Modelle funktionieren dabei schon drahtlos – sie werden entweder mit Batterien oder Solarzellen betrieben. Nachteile hat beides: So müssen Batterien regelmäßig ausgetauscht werden. Solarzellen können wiederum nicht versteckt am Fenster platziert werden, was die Ästhetik beeinträchtigt.

VµE Nachrichten, April 2012

Regallager checken sich selbst auf Standfestigkeit

Das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme IMS zeigt in Berlin zusammen mit der IWS Handling GmbH einen neuen Crash-Sensor für erhöhte Sicherheit in Lagerhallen. Üblicherweise werden die Stützen mit einer Art Luftkissen als Anfahrschutz versehen, der die Wucht von Stößen abfedern soll. In diese Schutzvorrichtung wurden Sensoren integriert, die den Druck innerhalb des Luftkissens messen. Wird ein Luftkissen angefahren, registriert der Sensor die dadurch verursachte Druckschwankung und meldet sie über eine Funkstrecke

ident, Januar 2012

RFID revolutioniert Logistik, Dokumentation und Wartung im Fassadenbau

LOGISTIK: Beim 87 m hohen Neubau der ADAC-Zentrale in München ist jedes Fassadenelement ein Unikat. Keines der 1152 Bauteile an dem im März eingeweihten Gebäude gleicht in der Farbkombination einem anderen. Zusätzlich zur elektronischen Stückliste wurde jedes Fassadenelement über RFID-Chips auf der Baustelle erfasst und am richtigen Ort eingebaut.

Nicht nur die Logistik von Herstellung, Anlieferung und Montage, auch die Lebenszyklus-Wartung des Fassade der neuen ADAC-Zentrale wird über RFID erleichtert: Sollten auch zehn mal Gläser, Beschläge oder Monieren beschädigt sein. Reicht der eingebaute Chip alle Informationen, um sofort das gewünschte Ersatzteil zu besorgen.

Die Josef Gartner GmbH, Gundelfingen, hat den geschossgroßen Hochhausbaustein einer 10 600 m² großen Fassade aus Aluminium und Glas verkleidet. Das farblich changierende Erscheinungsbild der Fassade entsteht aus insgesamt 22 verschiedenen NCS-Farbtönen (Natural Colour System) rund um das für den ADAC typische Gelb. Diese Farben verteilen die Fertigung der zweischaligen Fassade und den plastischen Eindruck des 16-stöckigen Gebäudes. Sie werden auf die Elemente aus Aluminiumprofilen und Blechen und Ruff-Stones per Siebdruck auf die Prallscheiben aufgetragen.

Die Vielzahl der Farbkombinationen, der Elementgrößen und Teile erforderte dabei eine besonders ausgeklügelte Logistik. Pro Stockwerk wurden zwölf verschiedene Elementtypen eingesetzt. Jedes Fassadenelement besteht wiederum aus elf das Äußere bestimmenden Bauteilen wie Sonnenschutz, Glas, beschichteten Profilen, Blechen etc. mit den spezifischen Farbkombinationen. Beim Zusammenbau der Elemente im Werk Gundelfingen erhielt jedes Element einen rund 5-Cent-großen RFID-

identifizieren, um die Position des Elements in der Logistikkette und beim Einbau exakt zu bestimmen sowie die Montage zu beschleunigen. Beim Einbau konnte der Monteur über sein Lesegerät kontrollieren, ob er das richtige Bauteil an richtigen Einbauort montiert. Im Display des Lesegeräts erschien entweder ein grünes Häkchen oder ein rotes Kreuz. Ohne RFID und anhand ausgedruckter Listen wäre eine Montage der 1152 verschiedenen Fassadenelemente höchst fehleranfällig gewesen. Gleichzeitig ermöglichten die RFID-Chips einen tagesaktuellen Überblick über den Stand der Fertigung und Montage.

Schneller Service und transparente Wartung

Im Vergleich zu einem aufgeklebten Barcode ist ein im Profil- oder Glasfalz unsichtbar angebrachter RFID-Chip achtungsbeständig und lebenslang haltbar. So können auch Wartung und Service für eine Fassade revolutioniert werden. Sollen beispielsweise das Glas oder ein ornamentaler Aufsatz des Fassadenelements beschädigt sein, kann der Facility Manager über ein Lesegerät die Nummer des Elements erfassen und mit Angabe des beschädigten Fassadenteils an den Fassadenbauer senden. Aufgrund der gespeicherten Stücklisten kann das Element sofort bestimmt und das richtige Ersatzteil bereitgestellt werden.

Lästiges manuelles Servicemitarbeiter mehr zum Kunden fahren, den Schaden vermessen und aufnehmen und dann erst in Stücklisten suchen. Das spart Zeit und Kosten beim Kunden wie beim Fassadenbauer.

Fassaden müssen in regelmäßigen Abständen gewartet werden, damit sie nach Jahrzehnten noch funktionstüchtig sind. Für diese Tätigkeiten sind Wartungsspezialisten von Gartner mit einem Tablet-PC mit USB-Reader ausgestattet. Sie können den RFID-Chip auslesen und die gesamten Wartungsarbeiten für das jeweilige Element elektronisch eingeben. So entsteht ein Wartungsjournal mit einer Rückmeldung und lebenslangen Dokumentation, das Kunden eine hohe Transparenz bietet.

Mittlerweile setzt Deutschlands führender Fassadenbauer, der weltweit über 1200 Mitarbeiter beschäftigt, diese Technik bei fast allen Projekten ein. So auch beim Neubau der Behörde für Stadtentwicklung und Umwelt, der gegenwärtig in Hamburg Wilhelmsburg entsteht und wie der ADAC-Bau von Sauerbruch Hutton Architekten entworfen wurde.

Gartner verkleidet den Neubau, der aus sieben Flachbauten mit einer Höhe von ca. 23 m und einem rund 50 m hohen Hochhaus besteht, mit einer rund 20 000 m² großen einschaligen Aluminium-Elementfassade. Auf die Elemente werden 8000 m² Keramikverschattungen mit 20 verschiedenen NCS-Farbtönen eruiert.

Aufgrund der geschwungenen Gebäudegeometrie gibt es gerade, konvex und konkav gebogene Steine, die mit verschiedenen Querschnitten und Farben zu kombinieren sind. Die Fassade ist höchst komplex, da von insgesamt rund 26 000 Keramikelementen 13 500 Steine verschieden sind. Ohne RFID wären die 2014 Fassadenelemente kaum zu realisieren.

Und auch die Logistik der besonders energieeffizienten und komplexen Fassadenelemente an 60 m hohem Verwaltungsgebäude der Bochar Diagnostics NG wurde über RFID-Chips gesteuert. Die 10 cm x 3 cm großen und 5 mm dicken Chips sind unsichtbar im Falz angebracht. Dieses Gebäude im Schweizer Barleuse kleidete Gartner mit einer Closed-Cavity-Fassade (CCF) ein, einer geschlossenen zweischaligen Fassade, die innen direkt und außen einfach verglast ist. Die CCF-Fassade ermöglicht den Einsatz hochtransparenter Gläser und hocheffizienter Sonnenschutzanlagen. Neben der Transparenz werden mit der von Gartner entwickelten CFF auch Energieeffizienz und Wirtschaftlichkeit verbessert. Beim Hochhaus in Rotkreuz erreicht die CCF-Fassade einen Uw-Wert von 0,91 und einen g-Wert von 0,31.

Qualitätssicherung und dokumentation

Der Einsatz von RFID-Chips und die Verknüpfung mit dem SAP-System gewährleistet eine exakte Bauteildokumentation über den gesamten Lebenszyklus eines

Fassade: RFID-Chips in jedem von 1152 Fassadenelementen an der neuen ADAC Zentrale behalten den Überblick.

VDI Nachrichten, April 2012

Blutzucker messen ganz ohne Blut

Ein winziger Chip im Auge soll Diabetes-Patienten weiterhelfen

▪ In allen Körperflüssigkeiten kann der Blutzucker gemessen werden. Der Chip könnte in drei Jahren auf den Markt kommen

SHARI LANGEMAX

Normalerweise tut jeder sein Bestes, sich möglichst nicht zu verletzen. Unversehrt zu bleiben ist ein natürlicher Instinkt. Manche Menschen müssen sich allerdings absichtlich verletzen, nicht selten mehr als zehn Mal täglich. Diabetes-Patienten lassen regelmäßig Blut, auch wenn es Überwindung kostet. Besonders de tut überhaupt nicht weh. Sie unangenehmer als das Tragen e takelinse", sagt Tom Zimmerm schäftsfeldleiter am Fraunhofer sammen mit seinen Kollegen i nen ultrakleinen bioelektrische entwickelt, der ganz einfach eingesetzt werden kann. Dort kontinuierlich die Konzentra Zucker – auch Glukose genannt Augenflüssigkeit.

Dass nicht nur Blut, sondern anderen Körperflüssigkeiten enthalten, wissen Mediziner s ge. Auch eine Korrelation konn nachgewiesen werden. „Der spiegel in der Augenflüssigke sich entsprechend dem Blutzu

Die Welt, September 2012

Meldungen

Biosensor erleichtert den Blutzuckertest

Baierbrunn (rgm) • Es ist der Traum vieler Diabetiker: Seinen Zucker zu messen, ohne sich stechen zu müssen. Wie das Apothekenmagazin „Diabetes Ratgeber" berichtet, haben Forscher des Fraunhofer-Instituts für mikroelektronische Schaltungen und Systeme in Duisburg einen winzigen Sensor entwickelt, der den Glukosespiegel in Tränenflüssigkeit oder Schweiß misst und das Ergebnis an einen Sensor funkt. Wann der Biosensor marktreif ist, steht noch nicht fest.

Magdeburger Volksstimme, Dezember 2012

Effizientere Chips durch Kupfer, Gold und Zinn sowie einen speziellen Galvanik-Prozess

ıer verbessern mithilfe von Gold, Kupfer oder Zinn und speziellen Galvanik-Prozessen die Funktionen v
itern. Auf diese Weise soll die Fertigung von mikroelektronischen Bausystemen leichter werden. Auch
ıdustrie könnte davon profitieren, berichtet die Fraunhofer Gesellschaft nun in einer Mitteilung. Ein mod

ATZ Online, Dezember 2012

Ein Sensor geht ins Auge, um den Innendruck zu messen

START-UP-PORTRÄT: Beim grünen Star – oder auch Glaukom – erhöht sich der Augeninnendruck derart, dass der Sehnerv geschädigt wird. Das Augenlicht erlischt schleichend. Das Gründerduo der Implandata Ophthalmic Products (IOP) GmbH will die Krankheit mit einem goldenen Sensorimplantat aufhalten, das den Druck im Auge kontinuierlich misst und die Daten nach außen funkt.

Nach und nach engt der grüne Star das Blickfeld immer weiter ein. Glaukom-Patienten wissen, dass ihre Perspektive völlige Dunkelheit ist. Erhöhter Augeninnendruck schädigt ihren Sehnerv. Für behandelnde Ärzte ist die Krankheit schwer in den Griff zu bekommen. Der Augeninnendruck lässt sich zwar von außen messen, doch solche punktuellen Datenerhebungen lassen der Krankheit viel Raum, ihr zerstörerisches Werk im Verborgenen fortzusetzen.

Diesen Raum wollen die Gründer der der Implandata Ophthalmic Products (IOP) GmbH aus Hannover, Max G. Ostermeier und Stefan Meyer, mit einer ins Auge implantierten Sensorik einengen. Der Chip zwischen Iris und Linse soll am Ort des Geschehens rund um die Uhr Druckverläufe aufzeichnen. Augenärzte können ihre Therapie so exakter auf den Patienten abstimmen und besung stimmt und wie weit die Therapietreue des Patienten geht.

Der am Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme entwickelte und auch dort gefertigte ASIC – sind Druck- und Temperatursensoren, Signalwandler und -prozessoren, das Energiemanagement sowie eine Funkeinheit vereint, die sämtliche Messdaten auf ein Handgerät überträgt. Dieses Gerät kann der Patient alleine bedienen und die gesammelten Daten direkt an den Rechner des behandelnden Arztes senden. Während der Datenauslese versorgt das Handgerät, das in etwa so groß wie eine TV-Fernbedienung ist, das implantierte Sensorsystem mit Strom.

„Um den Eingriff für Patienten klein zu halten, ist unser Implantat gefaltet", erklärt Ostermeier. Ein 2 mm kleiner Schnitt genügt, um es ins Auge einzubringen und dort zu entfalten. Nach Möglichkeit soll das zeitgleich mit dem Einsetzen künstlicher Linsen passieren, die bei Patienten mit grauem Star Standard sind. Hintergrund: Oft gehen grauer und grüner Star miteinander einher. Und weil die künstlichen Linsen flacher sind, als die natürlichen, bleibt genügend Platz für die Druckmessung der Hannoveraner.

Während die Gründer die ASICs am Duisburger Fraunhofer-Institut fertigen lassen, übernimmt eine EADS-Tochter die Verbindung mit der Spule und die Einbettung des Systems in Silikon. Nur die Endkontrolle und Funktionstests der

Da das Implantat anfangs gefaltet ist, genügt ein

2 mm

kleiner Schnitt, um ihn ins Auge einzubringen

Chip ist kaum 6,6 mm dick und findet im unteren Drittel einer runden Goldspule von 11,3 mm Durchmesser Platz. Diese

Augenärzte gewinnen dank der IOP GmbH wertvolle Einblicke in die Augen ihrer Patienten. Sensor und Lesegerät ermöglichen unkompliziert die stetige Kontrolle des Innendrucks.

köpfigen Team um Geschäftsführer Ostermeier und Elektrotechnik-Ingenieur Meyer. Für die beiden ist die 2010 gegründete IOP GmbH schon der zweite Versuch, die Glaukom-Sensorik zu reali-

selbst schon zwei Medizin- und Biotech-Start-ups zum erfolgreichen Exit geführt hat. Beim IOP-Vorläufer MesoTec misslang das, weil dem Lead-Investor 2006 die Pleite ausging.

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VDI Nachrichten, Oktober 2012

Das Netz der kleinen Dinge

Internet Ein neuer Schub des digitalen Wandels beginnt die Welt zu verändern. Nicht mehr nur Medien werden intelligenter, sondern unsere ganze Lebensumgebung. Die globale Feinverteilung der Informationsströme reicht von kluger Kleidung bis zum Fensterglas mit automatischer Privatsphäre. Von Peter Glaser

Stuttgarter Zeitung, Dezember 2012

Fachkräftemangel in der Pflegebranche

Beim **Tag der Gesundheitswirtschaft** am 22. Oktober geht es um den steigenden

(RP) Der Personalbedarf in der Pflegebranche nimmt massiv zu. Allein in Nordrhein-Westfalen werden bis zum Jahr 2030 etwa 40 000 Fachkräfte fehlen. Diese Entwicklung wirkt sich unmittelbar auf das Leben von pflegebedürftigen Menschen aus. Die Niederrheinische Industrie- und Handelskammer Duisburg-Wesel-Kleve richtet deshalb zusammen mit den IHKs in Nordrhein-Westfalen den „Tag der Gesundheitswirtschaft" am 22. Oktober, 17 bis 20 Uhr, im Fraunhofer-inHaus-Zentrum, Duisburg, aus.

Vertreter aus Wirtschaft, Wissenschaft und Politik diskutieren dann über mögliche Ansätze gegen den drohenden Fachkräftemangel. Unter anderem wird Ulrike Flach, Staatssekretärin im Bundesgesundheitsministerium, die Haltung

Die Veranstaltung beschäftigt sich vor allem mit zwei zentralen Herausforderungen, die die personelle Entwicklung in der Branche maßgeblich prägen werden: Technisierung und Mitarbeiterbindung. Die zunehmende Technisierung, beispielsweise durch Hilfs- und Assistenzsysteme, kann das Arbeiten zwar erleichtern, gleichzeitig aber auch die Pflegenden überfordern. Auch die Gefahr einer Entfremdung vom Patienten spielt hier eine nicht zu unterschätzende Rolle. Darauf nimmt die Veranstaltung mit verschiedenen Vorträgen und Diskussionsrunden ebenso Bezug wie zu der Frage, wie sich Pflegepersonal langfristig an ein Unternehmen binden lässt.

Weitere Informationen und Anmeldung für Unternehmen bei Ste-

Rheinische Post, Oktober 2012

Das Haus denkt mit

Zukunft ist, wenn die Waschmaschine den Klempner ruft und das Fenster weiß, wann es lüften muss

Von Ulla Berg

Deutschlands klügstes Haus steht in Duisburg. Die Gegend ist ruhig und grün, Wohngebäude auf der einen Straßenseite, Universitätsinstitute auf der anderen. Von außen fällt das weiß gestrichene

und Bügeleisen automatisch aus, die Heizung fährt herunter und offen stehende Türen und Fenster werden geschlossen." Möglich wird dies durch eine Vielzahl winziger Sensoren und Motoren, die per Funk Befehle austauschen und umsetzen.

Rückzug und Ruhe

Smart-Home-Missionare wie Klaus Scherer haben es nicht leicht mit dem modernen Menschen und seiner urmenschlichen Sehnsucht nach Rückzug und Ruhe. Aber letztendlines trifft er auf

rung, die älteren Menschen das Verweilen in der eigenen Wohnung ermöglichen soll. Wie Überwachung mit größtmöglicher Wahrung der Privatsphäre kombiniert werden kann, lässt sich im InHaus 2 besichtigen. Da gibt es zum Beispiel die Spezialküche, die registriert, wenn je-

Frankfurter Rundschau, Juni 2012

Kraftwerk im Keller

Neue Anlagen koppeln die Stromerzeugung mit der Wärmegewinnung

Wittigal Behr

Essen. Viele Hausbesitzer haben mit ihrer Solaranlage ein eigenes Kraftwerk auf dem Dach. Effizienter für eine Energiewende ist nach Ansicht vieler Experten aber ein Miniheizkraftwerk im Keller. So wie sich die kombinierte Erzeugung von Strom und Wärme in Großkraftwerken bewährt hat, soll in stärkerem Umfang diese Kraft-Wärme-Kopplung (KWK) auch im kleinen Maßstab realisiert werden. „Kleine KWK-Anlagen können gegenüber herkömmlichen Kraftwerken bis zu 33 Prozent Energie und bis zu 16 Prozent CO_2 einsparen", erläutert Bernhard Hörsgen von der Arbeitsgemeinschaft für sparsamen und umweltfreundlichen Energieverbrauch. Nach den Vorgaben der Bundesregierung soll bis zum Jahr 2020 ein Viertel des Strombedarfs aus Anlagen mit gekoppelter Strom- und Wär-

Vaillant baut Miniblockheizkraftwerke. Foto: Schmitte

werke verabschiedet. Gemeinsam mit dem Heiztechnikhersteller Vaillant ist RWE in das Geschäft mit Minikraftwerken für zu Hause eingestiegen. RWE eifert damit dem Ökostromanbieter Lichtblick nach, der ein ähnliches Konzept mit dem Autokonzern Volkswagen anbietet.

In den Blockheizkraftwerken Biogas entsteht mechanische Energie, die einen Generator zur Erzeugung von Elektrizität antreibt. Die gleichzeitig produzierte Wärme kann genutzt werden, um das Gebäude zu heizen und das Wasser für Bad und Küche zu erwärmen. RWE hat zusammen mit der Fraunhofer-Gesellschaft Duisburg eine Controlbox entwickelt, die die Anlage nach dem Strom- und Wärmebedarf des Kunden steuert. Außerdem wird sie darauf ausgelegt, künftig überschüssigen Ökostrom aus dem Netz in Form von Wärme zu speichern.

Diese Heizkraftwerke eignen sich für Kunden mit einem Wärmebedarf ab 60 000 Kilowattstunden pro Jahr. Die Investitionskosten liegen bei 40 000 Euro. Ab dem kommenden Jahr sollen auch kleinere Anlagen speziell für Einfamilienhäuser angeboten werden. Mit einer KWK-Anlage im Keller lassen sich nach Darstellung der Arbeitsge-

Neue Ruhr Zeitung, Januar 2012

APPS FÜRS HAUS

Die Deutsche Telekom begibt sich in einen neuen Markt: Sie will möglichst viele Hausgeräte vernetzen – und hofft, nach Vorbild von Apples iPhone eine ganz neue Plattform für Software-Anwendungen zu begründen. Noch fehlen allerdings die Partner.

Was haben sich Jalousie, Fernseher, Handy, Heizung und Beleuchtung zu sagen? Bisher eher wenig, denn zwischen Unterhaltungselektronik, Telekommunikation und Haustechnik herrscht eine babylonische Verwirrung an Standards und Protokollen (siehe TR 9/2009, S. 70). Nun will die Deutsche Telekom aufräumen. Ein System namens Qivicon soll die Bereiche vernetzen, um Energie zu sparen, Sicherheit und Bequemlichkeit zu verbessern und um ältere Menschen zu unterstützen. Es soll zu einem nicht näher benannten Termin Ende des Jahres auf den Markt kommen.

Qivicon basiert auf einer kleinen Box, die prinzipiell mit

deren Sache. Die Partner zahlen für jedes Programm, das ein Endkunde auf der Qivicon-Plattform installiert, eine Gebühr an die Telekom.

Die Telekom hofft, dass auf diese Weise eine Community aus unabhängigen Entwicklern entsteht, die ihre Kreativität in das System einfließen lassen und ganz neue Ideen finden, das Orchester der Haustechnik zum Klingen zu bringen. Wenn sich die richtigen Leute begeistern lassen, könnte das tatsächlich funktionieren: Beim Handy hatte sich vor wenigen Jahren schließlich auch niemand vorstellen können, dass die eingebaute Kamera einmal zum Bezahlen dienen würde (siehe TR 6/2012, S. 26).

Klaus Scherer, Leiter des Fraunhofer inHaus-Zentrums in Duisburg, hält Qivicon für einen Schritt in die richtige Rich-

Technology Review, Juni 2012

Sicherer wohnen

Eine intelligente Wohnumgebung für Senioren wird zurzeit in Darmstadt erprobt. Dabei melden z. B. Sensoren, wenn jemand hinfällt, beim nächtlichen Aufstehen schaltet sich das Licht von selber an, ein Sensorhemd misst den Herzschlag. Das Softwareprogramm für mehr Sicherheit wurde vom Fraunhofer-Institut entwickelt. Es soll individuell angepasst werden und einen „akzeptablen" Preis haben.

B.Z., März 2012

Lichtsysteme und ihre Wechselwirkungen

BELEUCHTUNG: Mit der Entwicklung neuer Beleuchtungssysteme wie LED und OLED bieten sich auch neue Möglichkeiten der Lichtsteuerung an. Licht kann gezielt eingesetzt werden, um menschliches Befinden, Leistungsfähigkeit, Konzentrationsvermögen und Aufmerksamkeit zu beeinflussen.

VDI Nachrichten, Düsseldorf, 27. 4. 12, ve

Halbleiter-Lichttechnologien (SSS: Solid States Lighting) wie LED (Light Emitting Diodes) und OLED (Organic LED) erzeugen Lichtstrahlungen aus Halbleiterelementen unter Einwirkung elektrischer Energie. Sie beingen mit ihren gegenüber herkömmlichen Lichttechnologien erweiterten Eigenschaften eine Reihe neuer technischer Optionen in die Gestaltung von Lichtsystemen in Raum und Gebäude, z. B. höhere Effizienz und farbiges Licht. Sie ermöglichen aber auch neue Wechselwirkungen mit Menschen, anderen Lebewesen, Pflanzen, Objekten und Materialien.

mus ist mit der Helligkeit und der spektralen Zusammensetzung des Sonnenlichts von Sonnenaufgang bis Sonnenuntergang synchronisiert. Der Einfluss des Sonnenlichtverlaufs auf den Schlaf-Wach-Rhythmus über den Tag bewirkt ausgehend von den Augen als Sensoren die verstärkte oder gebremste Ausschüttung von Melatonin (Schlafhormon). Generell unterstützen variable Lichtsysteme den natürlichen Rhythmus des Menschen. Tageslichtweiße Beleuchtung aktiviert (5600 Kelvin (K)); warmweißes Licht entspannt (3000 K).

Bei Versuchen des Uniklinikums Hamburg-Eppendorf (nach www.licht.de) gab es z. B. folgende Ergebnisse: Eine Schulklasse wurde über 10 Monate drei unterschiedlichen Lichtprogrammen für „Aktivieren" (12 000 K, 650 Lux), „Konzentriertes Arbeiten" (6000 K, 1000 Lux) und „Beruhigen" (2700 K, 300 Lux) ausgesetzt. Das Ergebnis war, dass die Fehlerquote bei den Arbeitsaufgaben um 45 % gegenüber einer Standardbeleuchtung sank, das Leseverständnis und die Lesegeschwindigkeit um 30 % stiegen und die motorische Unruhe in 8 min um 75 % gesenkt wur-

Völlig neue Möglichkeiten wird es mit der OLED-Technologie geben (Organic LED), die z. B. ein flächiges Licht an Wänden und Decken von Räumen ermöglicht. Licht wird dann ein nicht mehr dinglich fassbarer Bestandteil von Räumen sein.

KLAUS SCHERER

▸ www.inhaus.fraunhofer.de

Der Autor ist Geschäftsführer des Fraunhofer-inHaus-Zentrums für Intelligente Raum- und Gebäudesysteme, Duisburg.

„Intelligente Lichtsteuersysteme werden sich automatisch optimierend an Orte, Personen und Aktivitäten anpassen."

Klaus Scherer, Geschäftsführer des Fraunhofer-inHaus-Zentrums für Intelligente Raum- und Gebäudesysteme, Duisburg

VDI Nachrichten, April 2012

Smart wohnen: Wenn sich das Haus ganz bequem aus der Ferne steuern lässt

Das Haus der Zukunft weiß, wann welches Familienmitglied nach Hause kommt und steuert entsprechend Heizung und l
Fähigkeit der „Smart Buildings".

Rheinische Post, Januar 2012

Abschied von Mr. InHaus

Fraunhofer Quersumme, April 2012

Wohnen in der Zukunft - WDR Köln - Planet Wissen Extra: Technik für die Zukunft - 09.08.2012 15:19

Summary

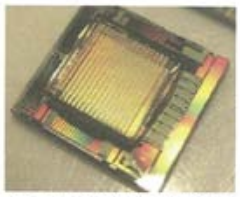
Planet Wissen sendet 3 Beiträge über Fraunhofer:
1. ähnlich wie "Wohnen in der Zukunft - Deutschlandfunk - Programm - 08.08.2012 18:40"
2. Zum Thema "Future Hotel" zeigt Britta Hennecken vom Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme IMS dem Journalist das Hotelzimmer der Zukunft. Dieser Raum wurde im Fraunhofer-inHaus-Zentrum in Duisburg entwickelt.
Sie erklärt die besondere LED-Lichtkonstellation, sowie die virtuellen Bedien-Tools für Schlaf-und Badezimmer der künftigen Gäste.
3. Sebastian Hantscher von der Abteilung Sensorsysteme für Sicherheitsanwendungen des Fraunhofer-Instituts für Hochfrequenzphysik und Radartechnik FHR schildert seine Arbeit an einem neuen Personenscanner für Sicherheitssysteme an Flughäfen etc. Dieser Detektor ermittelt anhand von elektromagnetischen Wellen, ob

WDR Köln, August 2012

Bildsensor:

Einzelne Photonen in rascher Folge nachgewiesen

Das Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme (IMS) in Duisburg hat einen hochempfindlichen Bildsensor auf Basis der CMOS-Technologie vorgestellt, der auf dem Chip Avalanche-Fotodioden integriert, mit denen sich einzelne Photonen nachweisen lassen.



Mit dem Avalanche-Sensor-Chip lassen sich einzelne Photonen nachweisen, auch wenn sie im Pikosekunden-Abstand aufeinander folgen.

(Bild: Fraunhofer IMS)

Mit den „Single Photon Avalanche"-Fotodioden lassen sich einzelne Photonen auch dann nachweisen, wenn sie innerhalb nur weniger Pikosekunden aufeinander folgen. Die Pixel-Struktur ist damit erheblich schneller als die bisher verfügbaren Sensoren. Die Fotodioden nutzen den Effekt des internen Lawinendurchbruchs (avalanche). Die Ladungsträger werden durch die angelegte Spannung schlagartig über die Sperrschicht getrieben; der Signalimpuls ist ausreichend groß, um die nachfolgende Schaltung sicher anzusteuern. Im neuen Fraunhofer-Chip ist jedem Pixel ein digitaler Zähler zugeordnet, der die Durchbrüche und damit die Anzahl der eingetroffenen Photonen zählt.

Auf dem Sensor-Chip wurden Mikrolinsen aufgebracht (Bild), die das einfallende Licht für jedes einzelne Sensorelement auf die photoaktive Fläche fokussieren. Um die Verarbeitungsgeschwindigkeit möglichst hochzutreiben, wurden die nachfolgenden Schaltungen für die Bildverarbeitung mit auf dem Sensor-Chip integriert. Wegen der rein digitalen Arbeitsweise – jedes nachgewiesene Photon erzeugt einen Impuls – ist eine analoge Signalverarbeitung entbehrlich. Da dieser Sensor

Jedes einzelne Photon erfasst, werden Aufnahmen auch bei extrem schwachen Lichtquellen möglich.

Das IMS ht den Sensor im Rahmen des europäischen Forschungsprojekts MiSPIA (Microelectronic Single-Photon 3D Imaging Arrays for low-light high-speed Safety and Security Applications) entwickelt.

Elektronik, Januar 2013

Fliegende 3-D-Augen

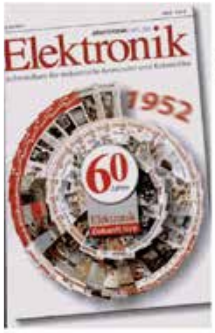
Ob als Einsatzhelfer bei Großveranstaltungen oder als hochauflösende 3-D-Vermesser von Straßenzügen: Intelligente Schwärme aus Flugrobotern eignen sich als universelles Werkzeug für Polizei, Krisenmanager oder Städteplaner. Für optimale Flugmanöver ohne Kollisionen sorgt ein spezieller 3-D-Sensor von Forschern des Fraunhofer IMS.

Wie auf Kommando steigt das Team laut surrend langsam in die Luft. Gut zwei Dutzend Flugroboter fliegen über Tausenden von Fußballanhängern. Aufgebrachte Fans haben das Spielfeld gestürmt und bengalische Feuer gezündet. Es kommt zu Schlägereien, Rauch verhindert die Sicht, es herrscht Chaos. Zu Hilfe eilt der Flugroboter-Schwarm.

Sensor löst höher auf als Radar

Gegenüber dem Radar, das mit Hilfe von reflektierten Echos Abstände von Objekten erfasst, bietet der Fraunhofer-IMS-Abstandssensor erhebliche Vorteile: »Die örtliche Auflösung ist sehr viel höher«, sagt Brockherde. »Ein Radar wäre bei dieser Nahfeldmanövrierung viel zu grob.« Auf eine Entfernung von bis zu 7,5 m erkennen die

VμE Nachrichten, Juni 2012



Sechs Jahrzehnte *Elektronik*

Im Laufe der sechzig Jahre ihres Bestehens hat die Zeitschrift Elektronik über viele technische Entwicklungen berichtet. In der Gründungsphase trat der Transistor auf den Plan, um in Wettbewerb mit der Elektronenröhre zu treten. So wie die fast ausgestorbene Röhre heute nur noch ein Nischendasein fristet, sind viele technische Errungenschaften gekommen und gegangen. Ein Streifzug durch die vergangenen 60 Jahre.

Eigenständige Zeitschrift

Die „erweiterte Ausgabe" ist zur eigenständigen und vollwertigen Fachzeitschrift *Elektronik* geworden, die erstmals monatlich erscheint – und mit auf 318 Seiten erweitertem Umfang. Mit der *Elektronik* Nr. 11/1955 erscheint erstmals ein Bild auf der Titelseite.

Memory Cards

Als kleineres, schnelleres und flexibleres Medium lösten die Memory Cards die Disketten ab. Die Speicherkarten liefen den konventionellen Speichermedien wie Harddisks oder Disketten schnell den Rang ab, da sie auch bei extremen Einsatzbedingungen wie hohe und niedrige Temperaturen, Erschütterungen, Staub und Feuchtigkeit zuverlässig arbeiteten. Positiv wirkte sich auch die Preisentwicklung auf den Siegeszug der kleineren Speicherkarten aus.

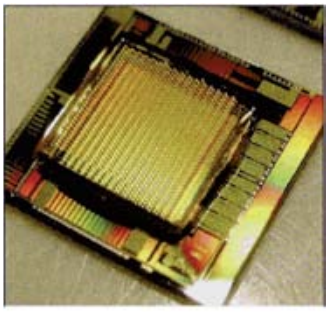
Sensoren in CMOS-Technologie

Da der Kostendruck immer härter wurde, versuchte man Sensorelemente und Signalaufbereitungselektronik auf einem Chip zu integrieren und auf bestehenden Produktionslinien zu fertigen. Die CMOS-Technologie machte es möglich, immer mehr Sensoreffekte in Silizium zu realisieren. Wegbereiter in der Forschung waren u.a. die Fraunhofer-Institute für Mikroelektronische Schaltung und Systeme in Dresden und Duisburg. Sie entwickelten u.a. monolithische Fotosensoren mit Signalauswertung, die in einem Standard-CMOS-Prozess hergestellt werden konnten.

Erste CMOS-Bildsensoren

In den 1970er und 1980er Jahren waren CCD-Bildaufnehmer die Platzhirsche im Bereich Bildsensoren. Das änderte sich, als das Fraunhofer-Institut für Mikroelektronik Stuttgart den ersten High Dynamic-Range-CMOS-Bildaufnehmer, kurz HDRC, vorstellte. Der CMOS-Bildsensor erreichte eine Helligkeitsdynamik von 1.000.000 : 1 (CCD: 4.000 : 1) und konnte bis zu 400 Vollbilder/s auslesen, mit der einstellbaren Bildgröße waren sogar über 1.000 Bilder/s möglich. Zum Vergleich: Übliche Videorecorder schafften damals 25 bis 60 Bilder/s.

Elektronik, Juni 2012



Die Jagd nach dem Photon

Bei extrem wenig Licht kommt es auf jedes einzelne Photon an. Fraunhofer-

Elektronik Praxis, Dezember 2012

Die 25. „Vision“ - Weltleitmesse für Bildverarbeitung

Als 1996 die „Ident/Vision“ mit nur noch 50 Ausstellern ihren Tiefpunkt erreichte, ahnte niemand, dass daraus schon in wenigen Jahren die Weltleitmesse für Bildverarbeitungstechnik hervorgehen sollte.

Vor einem Vierteljahrhundert hat kaum jemand das rasante Wachstum der Bildverarbeitungsbranche voraussagen können, deren Umsatz laut VDMA, Fachbereich Industrielle Bildverarbeitung, allein in Deutschland letztes Jahr die Rekordmarke von 1,5 Mrd. € erreicht hat. Das Anwendungsspektrum von bilderfassenden Systemen zum Messen, Prüfen und Überwachen ist nahezu explodiert und erschließt immer neue Applikationsfelder, insbesondere auch die nicht-industriellen. So liegen zum Beispiel noch große Potenziale in der Landwirtschaft, in der Wartung und Überwachung von Solar- oder Windkraftanlagen, in der Nutzung von Fahrerassistenzsystemen, in der Nahrungsmittelproduktion (etwa der Qualitätsbewertung von Obst und Gemüse) und im Umweltschutz.

„Es existieren noch viele interessante Wachstumsmärkte und es ist noch nicht abzusehen, welche Chancen die Zukunft noch bieten wird“, betont Christof Zollitsch, Geschäftsführer der STEMMER IMAGING.

Die Medical Discovery Tour wird 2012 fortgesetzt

Discovery Tour 2011 beteiligt. Aufgrund des Erfolges wird sie in diesem Jahr fortgesetzt.

CMOS-Bildsensoren sind zukunftsweisend. Stets kleinere Pixel und größere Bildsensorflächen sind gewünscht. Werner Brockherde, Entwicklungsleiter am Fraunhofer IMS, konstatiert: „Wir sehen aber auch den Trend hin zu anwenderspezifischen CMOS-Sensoren, weil Kamerahersteller Alleinstellungsmerkmale in ihren Produkten haben wollen.“

Unter dem Motto „One VISION“ sind in diesem Jahr (6. bis 8. November) erstmals alle Aussteller in der Hochhalle 1 unter einem Dach vereint. Mit über 21.000 m² ist dies die größte Messehalle der Messe Stuttgart.

„Es zeichnet sich ab, dass die VISION flächenmäßig weiter wachsen wird“, sagt Florian Niethammer erfreut, Projektleiter der VISION bei der Messe Stuttgart.

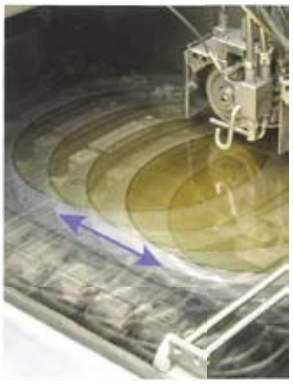
Lesen Sie online den ausführlichen Bericht: Wie es in Sindelfingen begann, warum fast das Aus für die Messe kam, wie die Vision schließlich zum Höhenflug ansetzte und nicht zuletzt, was die Besucher der VISION 2012 erwartet. // KU

Elektronik Praxis, Oktober 2012

Neues Bauelement bringt CMOS-Chips auf Trab

CMOS-Bildsensoren sind günstig in der Herstellung, sparsam im Verbrauch und einfach in der Handhabung. Doch bei lichtschwachen Anwendungen – etwa in der Astronomie – stoßen die Halbleiterchips bisher an ihre Grenzen: Große, in einer Matrix angeordnete Pixel erlauben keine raschen Auslesegeschwindigkeiten. Forscher des Fraunhofer IMS haben jetzt ein optoelektronisches Bauteil entwickelt, das diesen Prozess beschleunigt.

Die meisten handelsüblichen Digitalkameras, aber auch viele Mobiltelefone, sind heute mit CMOS-Chips ausgestattet. Deren Pixel sind zum Teil nur einen µm² groß. Für sehr lichtschwache Anwendungen, etwa in der Astronomie oder Röntgenfotografie, ist das jedoch zu klein. Dort muss der Lichtmangel durch eine größere Pixelfläche mit einer Kantenlänge von etwa 10 µm ausgeglichen werden.



Per High-Speed zum Ausleseknoten

Bei bisherigen CMOS-Sensoren steuern sogenannte Pinned-Photodioden (PPD) die Umwandlung von Lichtsignalen in elektrische Impulse. In den Chip eingebaut, sorgen diese optoelektronischen Bauelemente dafür, dass die durch das Licht erzeugten Elektroden zum Ausleseknoten diffundieren. Ein vergleichsweise langsamer Prozess, der für viele Anwendungen ausreicht. Über-

VµE Nachrichten, März 2012

Microlenses make 3-D endoscopes

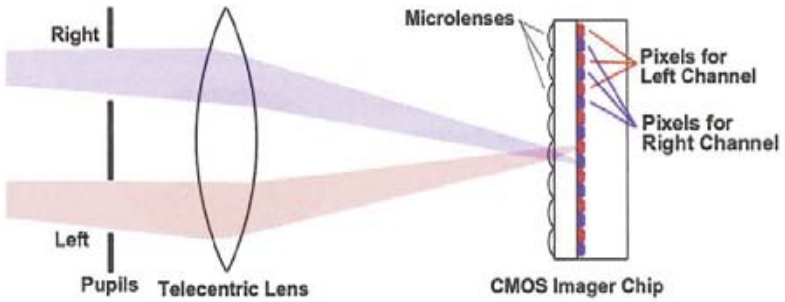
DUISBURG, Germany – A new image sensor that uses microlenses can transmit sharp 3-D images from inside the human body. The specially designed endoscope enables a surgeon to see minute details during operations, almost as though he were actually inside the patient's body.

The device's stereoscopic vision considerably simplifies the work of neurosurgeons and other specialists, who can now navigate a safe path through bodily tissues without the risk of collateral damage.

Researchers at Fraunhofer Institute for Microelectronic Circuits and Systems IMS developed the special microlenses in collaboration with partners from the European Union project Minisurg.

The secret of the 3-D endoscope system lies in the optical design of its CMOS sen-

Right: New microlenses, the surfaces of which are seen here through phase-shift interference microscopy, make it possible to transmit 3-D images from inside the body. Courtesy of Fraunhofer IMS. Below: A schematic representation of the 3-D microlens system.



Biophotonics, Januar 2013

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